iMajik: Making 1149.1 TAPs disappear and reappear in SoCs and 3D packages

CJ Clark, Intellitech Corp. Durham, NH
cclarkatintellitechdotcom

***Abstract* - The paper introduces a new protocol using just the TCK and TMS to transmit address and data called iMajik. iMajik is a method which 1149.1 based tools can use without modification to make 1149.1 TAPs appear and disappear, add compliance-enable without pins and broadcast commands to P1687 instruments. iMajik uses simple Test-Logic-Reset sequences with Run-Test-Idle to enable an on/off switch of various DFT capabilities. IEEE 1149.1 compliant TAP interfaces disappear to simple pass-through wires using the iMajik method. The sequences communicate an 'address' which enables one or more the TAP interfaces and a 'command'. iMajik may also have benefits for P1687 instrument chains and on-chip routing of the P1687 network.**

Keywords: TAP, JTAG, 1149.1, P1687, SiP, LSSD, SoC, 3D Package

I. INTRODUCTION

The IEEE 1149.1 standard allows subordination of the Test Access Port (TAP) through compliance-enable pins. This portion of the standard allows Level Sensitive Scan Design (LSSD) or muxed-scan IC test strategies to be used where the TAP operation may be temporarily switched on or off. It's a necessary 'evil', evil in the sense that it 1) adds one or more pins to the package that cannot be used for any other function 2) causes difficult to diagnose scan-path failures during board test when the TAP is thought to be operational but the compliance-enable pins are open or stuck-at due to a solder defect.

Compliance-enable pins have also been used by IC vendors to select a 'main' tap for the IC and 'hide' the other TAPs when multiple TAP'd cores exist in the design. This presents a shorter scan path for emulation or hides details that an IC vendor may not want to provide. Daisy-chained 1149.1 TAPs in a System-on-Chip (SoC) requires extra test clocks to shift through the cores which can affect test and emulation performance. Test data volume over 1149.1/JTAG continues to escalate especially for programming in-package FLASH in a 3D package. IEEE P1687 describes TAP operated on-chip instrumentation further increasing test data volume over the single full-duplex serial connection of IEEE 1149.1. Therefore reducing the number of registers and Test Clocks (TCK) required can improve performance.

As early as 1994, authors have described methods to deal with the limitations of the IEEE 1149.1 one bit BYPASS register and 32 bit DEVICE_ID register[1]. The problem at the time was that Multi-Chip Modules (MCM) contain TAP'd die and Boundary-Scan Description Language (BSDL) file for each device, but at the Printed Circuit Board (PCB) level the MCM must also present itself as single 1149.1 compliant device with a single BSDL. The IEEE 1149.1 working group was presented in the 1990s arguments for allowing these registers to be variable length, with the length defined by BSDL. Veteran DFT expert and original JTAG member (which later became the 1149.1 Working Group) Frans De Jong had presented on this very topic. This flexibility, which is allowed in any other 1149.1 register, was voted on but enough WG members at the time unfortunately voted it down. Work has been done since then for Single Inline Packages (SiP) and presented by De Jong, *et al* [2]. The approach uses an extra 'STDI' input on each die and connecting all of the STDI together to the main package Test Data Input (TDI). It's a nice approach to make the SiP appear to have one TAP. However, this approach doesn't help much to shorten the scan-chain for multi-core devices. The number of loads on TDI and STDI may also limit performance. Vermeulen[3], et al describe another method which requires a chip level TAP. This is also a good approach but requires one core or die to be designed specifically for a multi-TAP package. Like De Jong's approach, it doesn't help with TAP management and reducing TCK cycles for each IR and Bypass register and it can't be used to remove compliance enable pins.

The very inventive Lee Whetsel describes a TAP linking approach[4]. Lee has an impressive wall of patent plaques in his office. The TC2100 examiners joke that they hire at least one extra examiner just to handle all of the patents Lee can produce. The TAP linking approach can reduce the scan-chain TCK count in a coarse manner for each chain that is linked. It is limited as it requires a chip level or SiP package level die that has the TAP linker in it. It is a TAP itself so it cannot help with compliance enable pins. It also introduces additional register data bits in the scan path which tools must account for. Most FPGA and CPU emulation tool software don't support these types of linking devices due to the complexity and lack of standardization of how they operate. The linker doesn't help remove compliance enable pins. Whetsel also described an "Addressable Shadow Protocol" back in 1992 which transmits data using TDI and TCK in the Run-Test/Idle (RTI) state[5]. This doesn't work well for daisy-chains of TAP'd cores since TDI is not distributed to all of the targets, and it isn't useful in removing compliance-enable pins.

[1] Jarwala, Najmi T., "Designing Dual-Personality IEEE 1149.1-Compliant Multi-Chip Modules". ITC 1994: 446-455

[2] De Jong, Frans, Biewenga, Alex, "SiP-TAP: JTAG for SiP" ITC 2006., page(s): 1-10

[3] Vermeulen, Bart, Waayers Tom, Baker, Sjaak, "IEEE 1149.1-Compliant Access Architecture for Multiple Core Debug on Digital System Chips", ITC 2002

[4] Whetsel, Lee, IEEE 1500 meeting, http://grouper.ieee.org/groups/1500/dac97/p1500.pdf

[5] Lee Whetsel: A Proposed Method of Accessing 1149.1 in a Backplane Environment. ITC 1992: 206-216