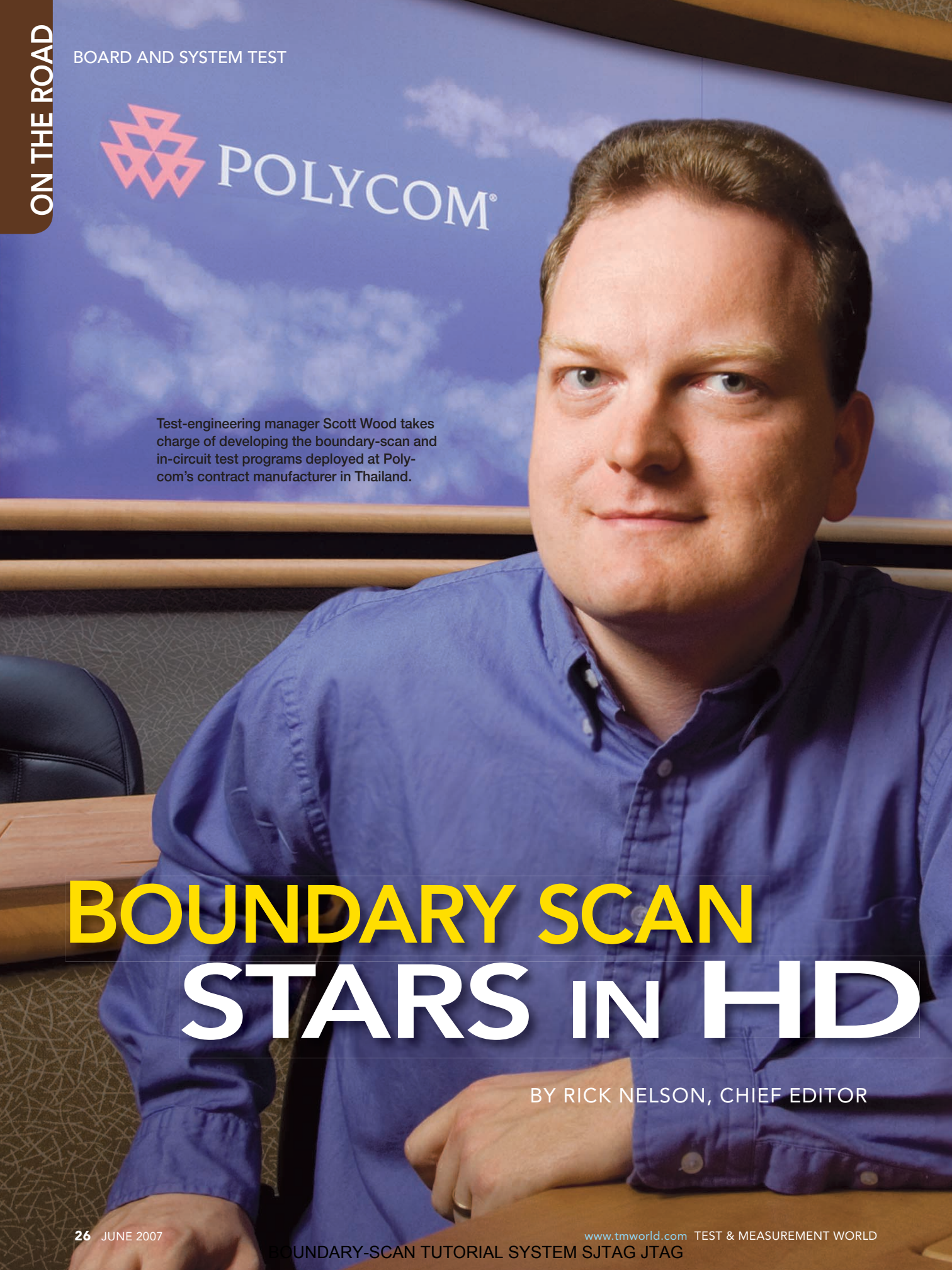


Test-engineering manager Scott Wood takes charge of developing the boundary-scan and in-circuit test programs deployed at Polycom's contract manufacturer in Thailand.

BOUNDARY SCAN STARS IN HD

BY RICK NELSON, CHIEF EDITOR

DAN BRYANT

CONFERENCING

Engineers at Polycom chose IEEE 1149.1 JTAG technology to ensure the testability of their company's new high-definition videoconferencing system.

AUSTIN, TX. Videoconferencing promises to revolutionize interpersonal communication in myriad applications. Although the concept is not new, recent advances are extending the technology well beyond the talking-heads format of formal business meetings. The audio and video qualities as well as the ability to track motion have become sufficiently sophisticated to open up new applications in real estate, manufacturing, medicine, and education.

One manufacturer that is devoted to expanding the capabilities of videoconferencing is Polycom. Here are just a few applications that were made possible by Polycom's new generation of HDX high-definition videoconferencing systems, which the company introduced last November:

- The Cleveland Museum of Art uses videoconferencing to make art and artifacts available outside the museum, to develop programs in conjunction with teachers across the US, and to teach a distance-learning three-credit semester-length university-level art course.
- Mote Marine Laboratory uses Polycom systems to present live, interactive distance-learning programs to students of all ages; the organization uses videoconferencing to project its 135,000-gallon shark tank in Sarasota, FL, to such far-flung locations as Fargo, ND.

• The Beth Melsky agency uses Polycom equipment to stage remote casting calls, allowing a director in Los Angeles, for instance, to audition an actor in New York.

ICT becomes insufficient

But when engineers at Polycom embarked on their development process for the new high-definition (HD) systems, they realized they would face some tough challenges. For example, when they began auditioning components for the systems, and when they began designing printed-circuit-board (PCB) stages on which these components would play, they knew their existing in-circuit test (ICT) strategy would no longer suffice.

Scott Wood, test-engineering manager, explained, "It was clear that chips and components and circuitry necessary to produce the high-definition video inputs and outputs would require very dense multilayer boards—there are probably five times as many components in our new product than were in the most complicated of our older products. So because of board complexity, it was clear that our traditional ICT wasn't going to work if we wanted to maintain the test coverage that we've had historically."

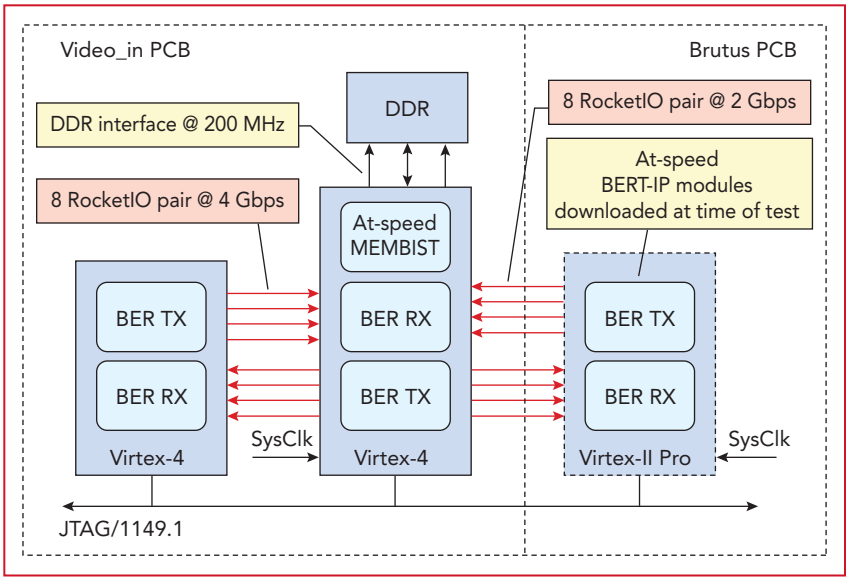
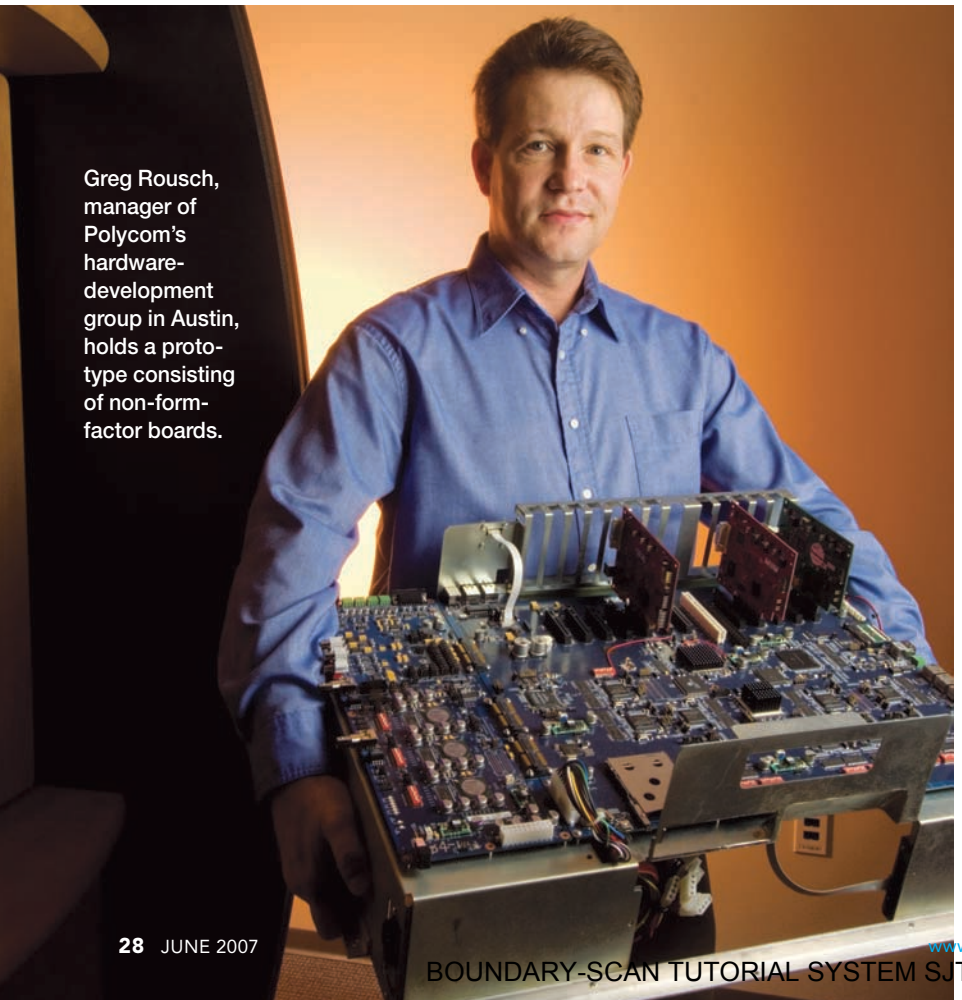


FIGURE 1. Intellitech's BERT-IP modules take the form of downloadable bit streams that configure built-in test structures within the Xilinx Virtex-II Pro and Virtex-4 FPGAs used on the Polycom boards.



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Greg Rousch, manager of Polycom's hardware-development group in Austin, holds a prototype consisting of non-form-factor boards.

Chief among the challenges would be the presence of high-density micro ball-grid arrays (BGAs) and other high-density solder-ball chips, as the bed-of-nails fixtures used on earlier-generation products could not provide the necessary levels of test coverage for these components. The engineers knew that they needed an alternative technology. Further, the difficulties would present themselves not just during high-volume production but also during development: Polycom's hardware engineers needed to supply their software-engineering counterparts with sufficient hardware prototypes to exercise the code under development.

Walter Haskell, senior staff engineer at Polycom, said that the HD system development began with what he and his colleagues call a "non-form-factor" board—one that's larger than the production boards ultimately used in the new system but, nevertheless, one designed to embody the new system's functionality. "Because of the complexity—we have so many processors and signals—the law of averages said that if we didn't have some good way of checking things out, we would be plagued with problems."

His recommendation? "I started thinking of boundary scan as an option."

Greg Rousch, manager of the hardware-development group, concurred. "Boundary scan has been out there for almost my whole career, but I had never

used it until we began this development effort. Up until then, we had just always used bed-of-nails test fixtures. Our layout team put dedicated test points down to support bed-of-nails ICT test fixturing, and that's just always been good enough. What has changed that are the high-density ball-grid-array packages, because it's very difficult to probe on a board and measure the soldering quality of a BGA package."

Rousch added that not only are board densities getting to the point where it's hard to place test points, but that even if board real estate is available, putting test points on high-speed nets can adversely affect signal integrity. Taking such factors into consideration, he explained, "When Walter came to me and said that he really felt we should be considering boundary scan for this product, I agreed."

Wood noted that Polycom continues to employ ICT for mixed-signal and other device test that's not amenable to boundary-scan, but he added that the Intellitech boundary-scan implementation Polycom chose—the Eclipse system—can test most of the digital portions of the boards, including high-speed RocketIO data lines carrying HD video signals at rates to 4 Gbps between field-programmable gate arrays (FPGAs) (**Figure 1**).

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Senior staff engineer Walter Haskell concluded that boundary scan would be the best option for testing the many processors and signals on Polycom's new high-definition videoconferencing systems.

Intellitech's RocketIO test capability is based on an at-speed BERT-IP test module that works in conjunction with Intellitech's Eclipse JTAG system. The BERT-IP module takes the form of a downloadable bit stream that configures built-in test structures within the Xilinx Virtex-II Pro and Virtex-4 FPGAs used on the Polycom boards. The configured built-in test structures include pattern generators, high-speed transceiver controls, and pattern receivers that enable the real-time detection and display of bit errors.

The Intellitech at-speed test function also enables indirect test of parameters such as clock oscillator jitter and DC/DC-converter noise as well as voltage levels that are not testable using standard JTAG capabilities. In addition, it can test DDR and RocketIO termination resistors, DC blocking capacitors on RocketIO differential lines, and the RocketIO lines themselves that don't include 1149.1 boundary-scan cells.

But for the regular analog components, Wood said, the team continues to rely on ICT. "Boundary-scan coverage gets us almost all the way there and allows us to do things that with ICT alone wouldn't be possible. But for those areas that boundary scan can't cover, we use a much more limited ICT fixture than we used to use to get near 100% coverage." *(continued)*

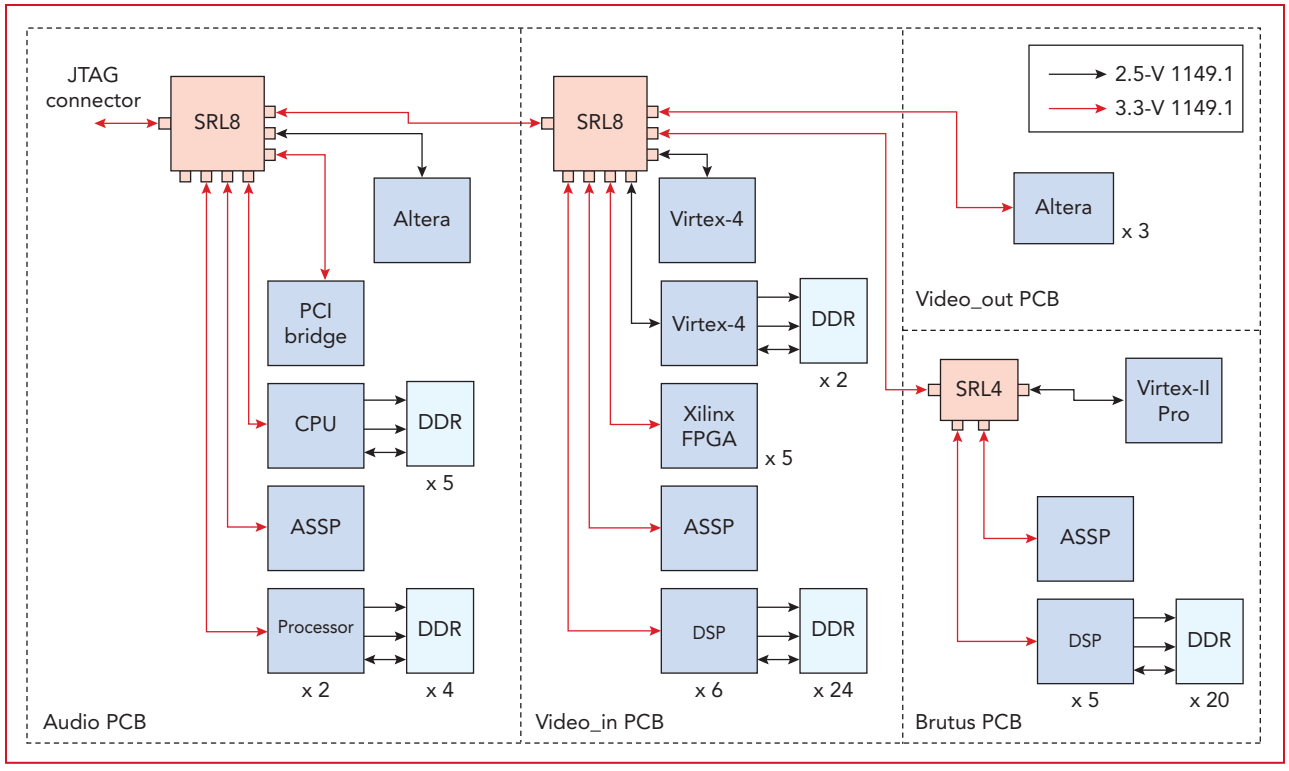


FIGURE 2. A Scan Ring Linker (SRL) on each board serves as a high-speed JTAG test-bus interface, linking secondary scan chains to a single IEEE 1149.1 external interface. A single JTAG connector enables multiboard test.

FPGA BER SERDES Bit Error Rate Test 1149.6

Simplifying boundary-scan I/O

In addition to the Eclipse system and BERT-IP, the Polycom team also made use of Intellitech's Scan Ring Linker (SRL)—a high-speed JTAG test-bus interface. The SRL links secondary scan chains into a single high-speed test bus connected to a single IEEE 1149.1 external interface.

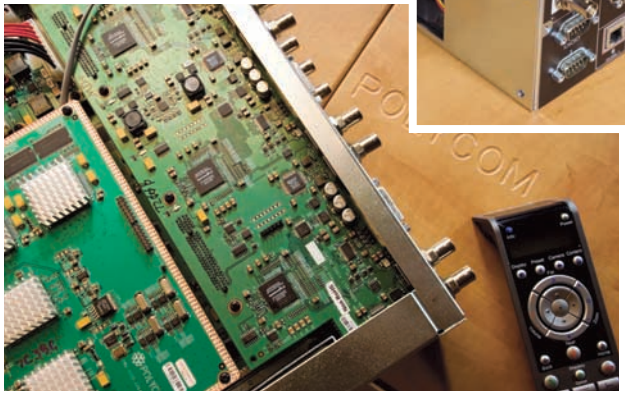
"Instead of having 10 or 15 different external scan-chain connectors and cables," said Wood, "the SRL lets us use one connector and cable per board to make our boundary-scan connections." The SRL also permits a single connector to enable multiboard tests, and it supports multiple voltage domains, as shown in **Figure 2**.

Wood said that in the future, he intends to take advantage of Eclipse's links to National Instruments' LabView—the program he has traditionally used to develop his manufacturing test programs. "Intellitech has a nice LabView interface to its boundary-scan software. We haven't implemented that yet, but when we do, it will further simplify our test deployment to our contract manufacturer."

When asked whether he had difficulty convincing his contract manufacturer's (CM's) engineers to employ boundary scan, Wood said, "The bottom line was when they saw the complexity of this product relative to the other products they had built, it was obvious to them, especially from a debugging perspective, that boundary scan was going to be invaluable. It was immediately obvious to them that this was the only way they were going to get access, so there wasn't any pushback. It saves them a lot of time, which is what they are most interested in—they need to be able to get high-quality products out the door that work. And when they don't work, they need to be able to quickly identify problems and fix them. Boundary scan helps them do that."

The Polycom engineers try to focus on design, shifting test responsibilities onto its CM. Speaking of the CM engineers, Wood said, "We have been working with this group for so long that we have a great working relationship with them." Rousch seconded that: "They are very competent test engineers—in fact, two of them, who are Thai citizens, trained at UT Austin. When we completed our test program, Scott literally just made a copy of it and went over to Thailand and set it up."

Nevertheless, said Wood, although the CM test engineers "can handle most ICT-related problems without having to get us involved too often, we are still in the beginning stage of using boundary scan, so they are still dependent on us to help resolve some issues they come across. But as more and more of our products start to use boundary scan, we will push more of the responsibility back on to them."



The many I/O channels (top) and the circuit-board density (bottom) of Polycom's HDX videoconferencing system made it necessary for the product's development team to augment in-circuit test with boundary scan.

DAN BRYANT

Boundary scan in prototypes

Wood's primary responsibility is production test, but boundary scan has been important to the Polycom team from initial prototype stages. Said Rousch, "We tried as hard as we could to have the boundary-scan test available on our very first prototype, which was a massive non-form-factor board."

Because boundary scan was new to the Polycom team, they delegated boundary-scan program development to Intellitech, providing Electronic Design Interchange Format (EDIF) netlists as input. Fortunately, said Rousch, "Intellitech did a good job of keeping up with us as far as having tests ready. As soon as our first board came off the assembly line here at a local assembly shop, [Intellitech applications engineer] Carl Nielsen flew down here and almost in real time was debugging his program and also finding bugs in our product at the very same time. It was a big help right during that first bring-up to use boundary scan as a design debug tool."

Asked about additional test challenges he faces, Rousch said, "My team develops all the board-level hardware for our products, but we have a whole floor of software engineers. Most of the magic is in the software, so we are critically dependent on the software team. My biggest test challenge is that the software team is running behind the hardware team, and we really need the software to fully exercise our hardware."

Haskell, the senior staff engineer, proposed a possible boundary-scan solution to this problem: "We would like to go further with boundary scan to where we can manually toggle some pins on a prototype board. In some instances we might think a pin should be in a certain state, but it's not—possibly because of software issues. If we could use boundary scan to toggle those pins, we could speed up our hardware debug while waiting for software updates."

Rousch noted that there is a flip side to the problem of hardware teams waiting on software: "Because there are so many software developers, we get a tremendous amount of pressure to make lots of copies of prototypes even before We've had a chance to completely debug them." Ideally, he said, the software engineers would be able to simulate their software running on the target hardware without actually having the target hardware available. "That's an old problem that's been around ever since I've been in the industry. If hardware technology

stayed static, the industry could catch up. But the hardware just keeps getting more and more complex. The modeling technology always lags, and for video designs, it never catches up."

In fact, Rousch said, in this respect, the industry has lost ground. "In the late '80s and early '90s, I worked for a medical equipment company, and we used to model complete boards—the chips were smaller, and there was a whole industry set up for supplying models for co-simulation environments. The simulations would run really slowly, but at least they would run. But in the last 10 or 15 years, everyone just gave up. The chips got bigger and more complex, and good models often weren't available, so board simulation fell apart. The only place we do simulation now is with FPGAs."

In addition to an effective co-simulation environment, Rousch has another item on his test wish list: "In general, digital video is very difficult to test. It takes an enormous amount of test vectors to really test digital video. If something could be done to give better coverage with less test time, we would always be looking for some innovation there."

Wood has his own wish list. In terms of OS support, he said, he would like to move away from Windows toward an open-source system. "As a rule in our organization, we use open-source software wherever possible." Most of Polycom's production line, he added, runs off Linux.

But the team is nevertheless satisfied with its initial boundary-scan experiences. Said Rousch, "We are absolutely going to continue using boundary scan." Added Wood, "Our first HDX product design was a huge leap. As we continue developing new products on an ever more accelerated cycle, we will be looking at ways to apply boundary scan even more effectively." T&MW

FOR FURTHER READING

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