SOLUTIONS FOR UNDETECTED SHORTS ON IEEE 1149.1 SELF-MONITORING PINS

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Abstract *– This paper presents the problem of undetected shorts on IEEE 1149.1 compliant self-monitoring pins. Unidirectional and bidirectional self-monitoring pins may contain sufficient series termination resistance and low enough voltage swings such that shorts between two pins become resistively isolated from the receivers and therefore are undetected during wiring interconnect tests. Potential solutions to mitigate the problem are offered.*

Keywords: 1149.1, Wire Interconnect, JTAG, shorts, hysteresis, Board Test, Boundary Scan

I. INTRODUCTION

A self-monitoring pin is a type of boundary-scan driver pin which can capture the logic level that the output drive buffer is driving. Figure 11-32, 11-33, 11-37, 11-40 and Figure 11-41 of the IEEE 1149.1-2001 standard illustrate conceptual compliant designs supporting self-monitoring pins[1].

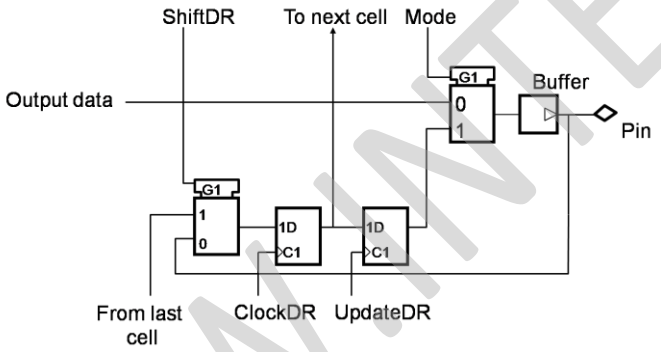

Figure 1. BC_10 type self-monitoring pin

A unidirectional two state output with self monitoring capability is shown in Figure 1. The logic value at the pin is captured prior to the SHIFTDR state and shifted out on TDO for analysis.

Pins with self-monitoring capability are preferred for board test as they improve fault diagnostics for 1149.1 driver to receiver interconnect tests. Figure 2 illustrates the self-monitoring pin A captures back a logic '1' when the net is open and pin B captures back a logic '0' when the net is shorted to ground. Without this self-monitoring capability, 1149.1 based tools will only see the constant logic '0' captured by the receivers on each net. Some 1149.1 software tools take advantage of the incorrect value seen by the driver to correctly diagnose the difference between a stuck-at fault on the net and an open on a net. This is an important distinction necessary to properly select between inexpensive or costly repair operations.

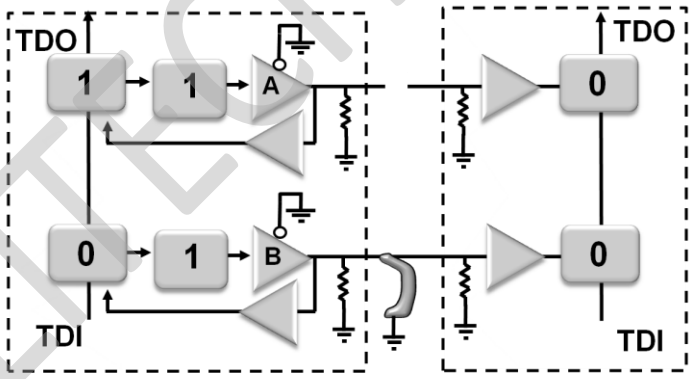

Figure 2. Difference of short-to-gnd and open

These types of self-monitoring pins are also capable of detecting shorts between nets that connect a Boundary-Scan device and a powered non-Boundary-Scan device or passive component such as a connector. Figure 3 shows a portion of a compliant IEEE 1149.1 device with three self-monitoring unidirectional outputs labeled A, B and C. Board level ATPG (Automatic Test Pattern Generation) tools would read the netlist and BSDL (Boundary-Scan Description Language) files for the ICs present to generate the test patterns. The board nets for A, B, and C would be each assigned a unique signature. During interconnect testing the ICs are loaded with the EXTEST instruction. When the test patterns are applied, the first bit of each net's unique signature is shifted in to the capture/shift flip-flop. In this case 1-0-1 is shifted in representing the LSB of the unique signatures for A, B and C. On the falling edge of TCK, while leaving the UPDATE-DR state, the values are moved to the update register and the logic value is driven by the output buffer. When the next bit of the unique signature, a 0-1-1 is to be shifted in, the tap controller must go through the CAPTURE-DR state.

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