

# **New IEEE Std. 1149.1-2013 lowers industry costs through test re-use from IP to Systems**

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**Chairman, IEEE 1149.1-2013**



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# IEEE 1149.1-2013 Executive Summary

- Standardizes a plug-n-play test interface to on-chip IP

## Mission IP

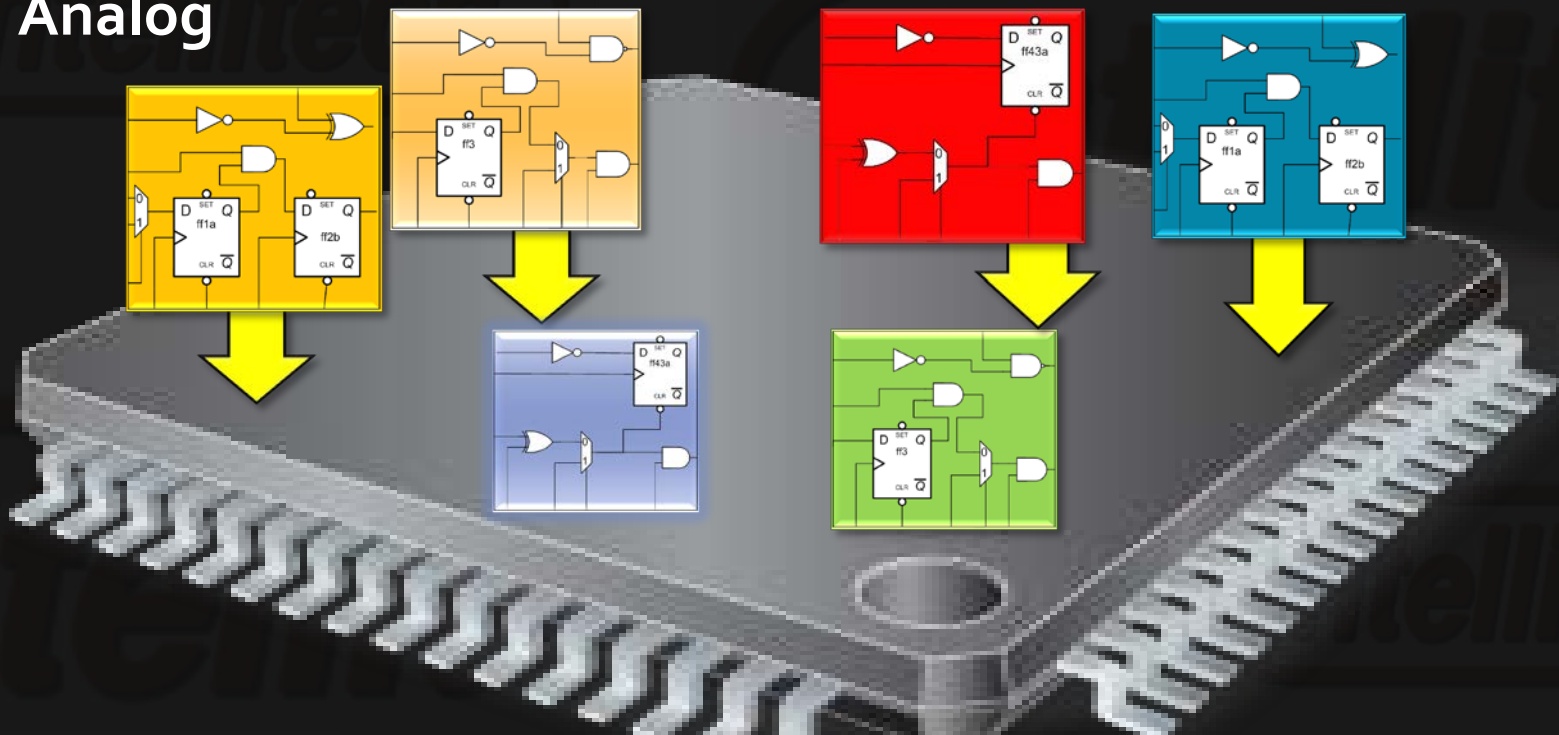
CPU  
 DSP  
 Memory  
 Analog

Graphics  
 Connectivity  
 Etc.

## Infrastructure IP

Embedded Test  
 Memory BISR  
 SerDes BIST

Voltage/Temp  
 Security  
 Process monitors



See Yervant Zorian: "Infrastructure IP for SoCs" and "What is Infrastructure IP?"  
 BIST = Built In Self-Test    BISR = Built-in Self-Repair

# 1149.1-2013 adds depth to the other half of the standard

## - Standard Test Access Port and Boundary Scan architecture

"Boundary Scan" has always been a misnomer, it's only a part of the standard.

Standardization now available for all internal JTAG registers via the Test Access Port

Hierarchical descriptions of on-chip IP

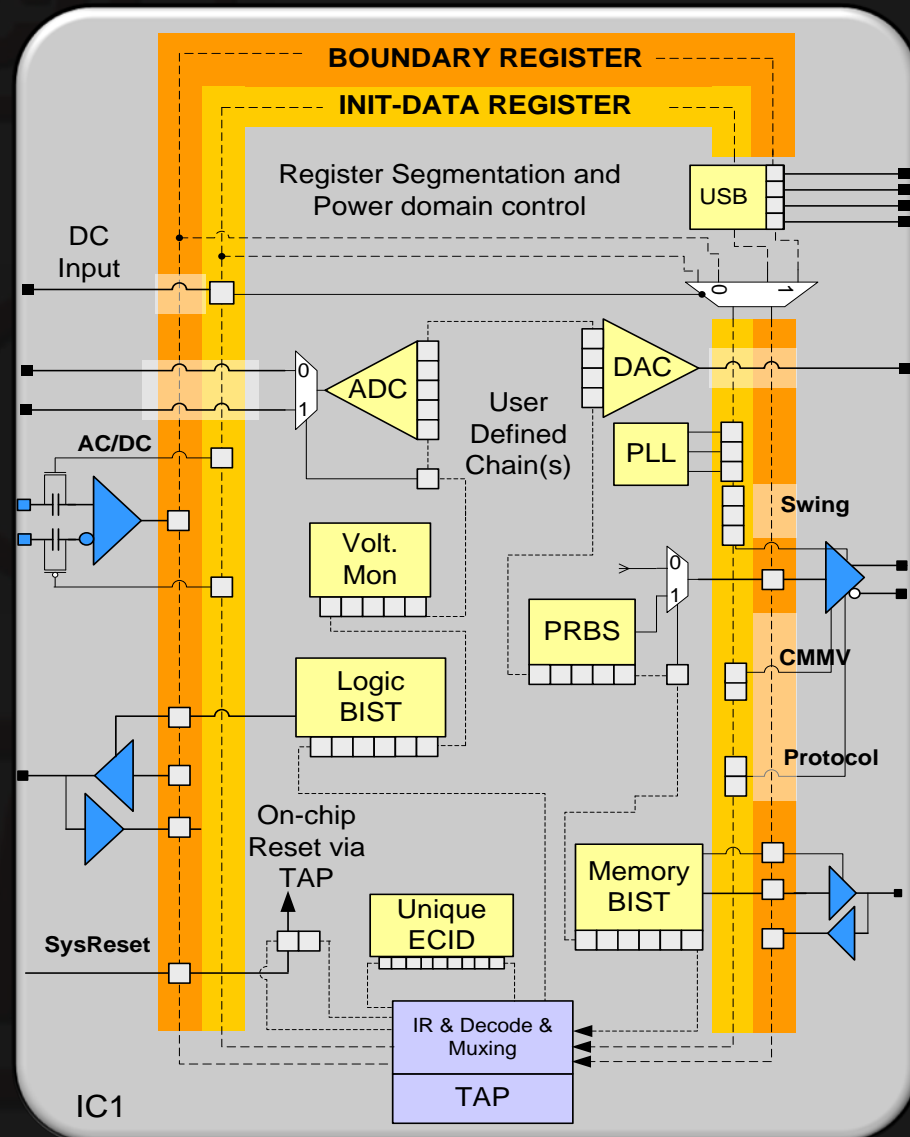
Hierarchical operational language for On-chip IP

Synergy with IEEE 1500 and IEEE 1801

- re-use popular IEEE 1500 structures

- TDRs can cross power domains

444 Pgs vs. 208 pgs in 1149.1-2001



# Or...two thirds of the defined scope!

## 1. Overview

### 1.1 Scope

This standard defines test logic that can be included in an integrated circuit to provide standardized approaches to:

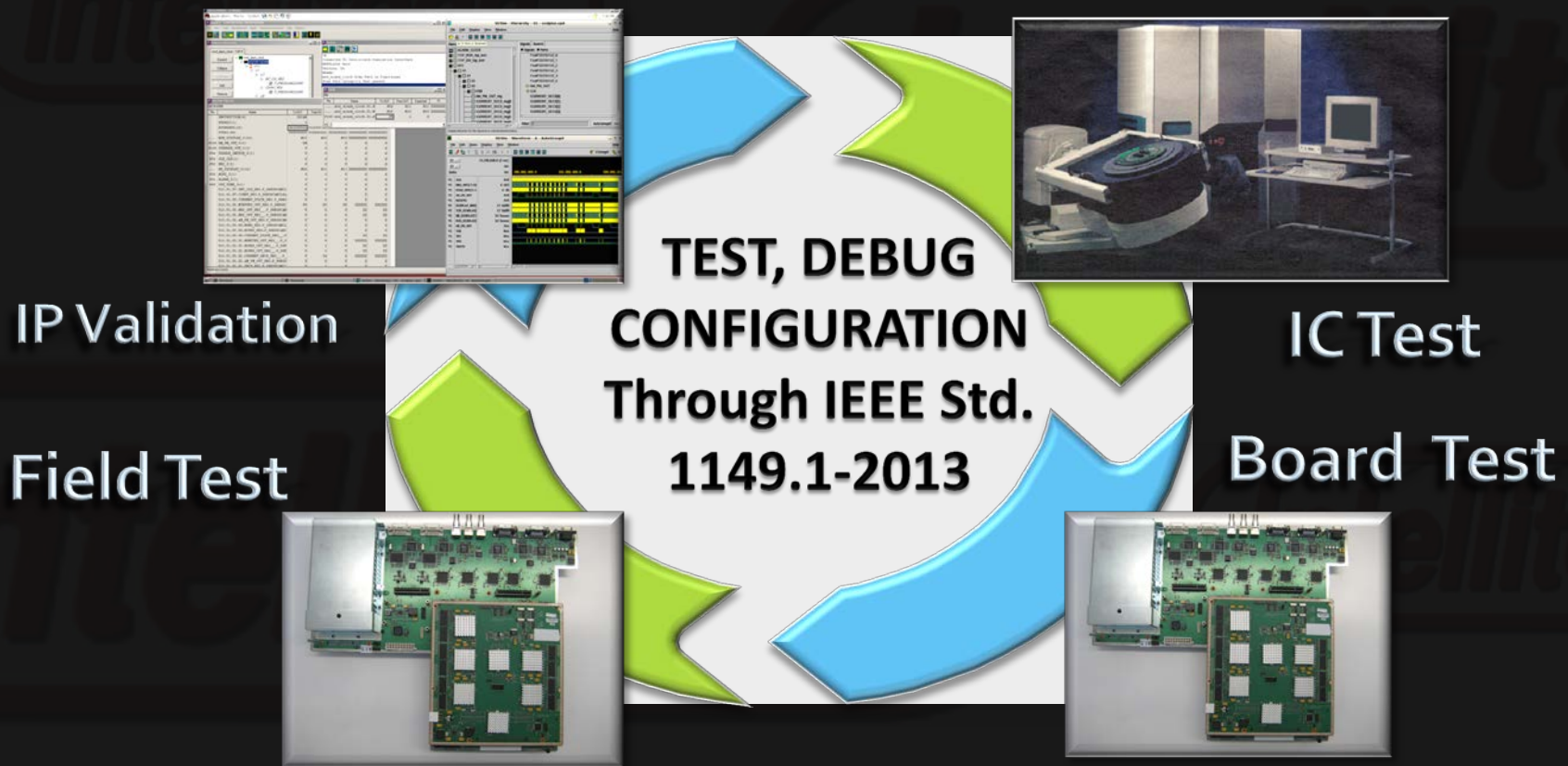
- Testing the interconnections between integrated circuits once they have been assembled onto a printed circuit board or other substrate
- Testing the integrated circuit itself
- Observing or modifying circuit activity during the component's normal operation

The test logic consists of a boundary-scan register and other building blocks and is accessed through a test access port (TAP).

# IEEE Std. 1149.1-2013 lowers industry costs by enabling test re-use through all phases of the IC life-cycle

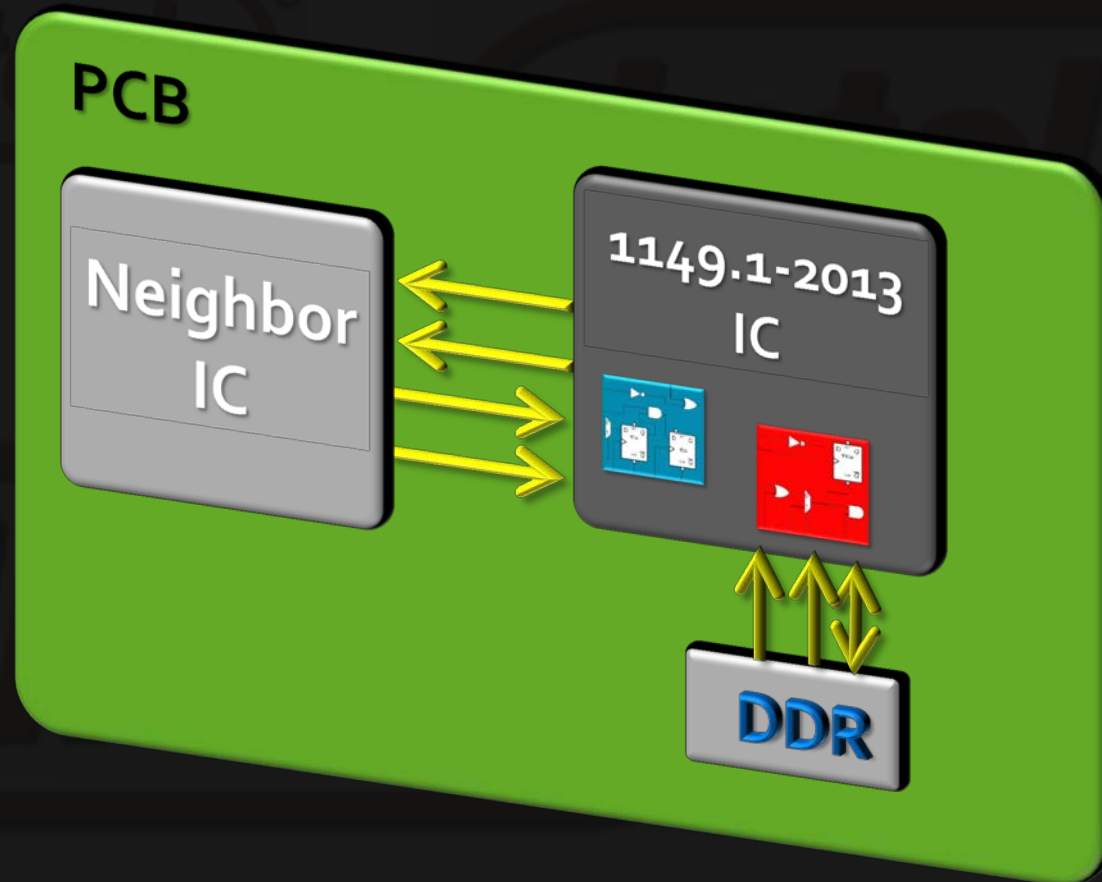
- Specifies best practices for Infrastructure IP test interfaces
- Specifies rules for describing IP operation
- Enables one description to be used in all test stages
- Enables defect correlation between system failures and IC ATE

**Note: doesn't require production IC test through TAP**



## 1149.1-2013 enables ecosystem tests

- Test the interactions of the IC with supporting PCB components
- Ecosystem tests - valuable for IC customer/system integrator
- Valuable for IC vendor to exonerate/validate to the customer that the IC is working

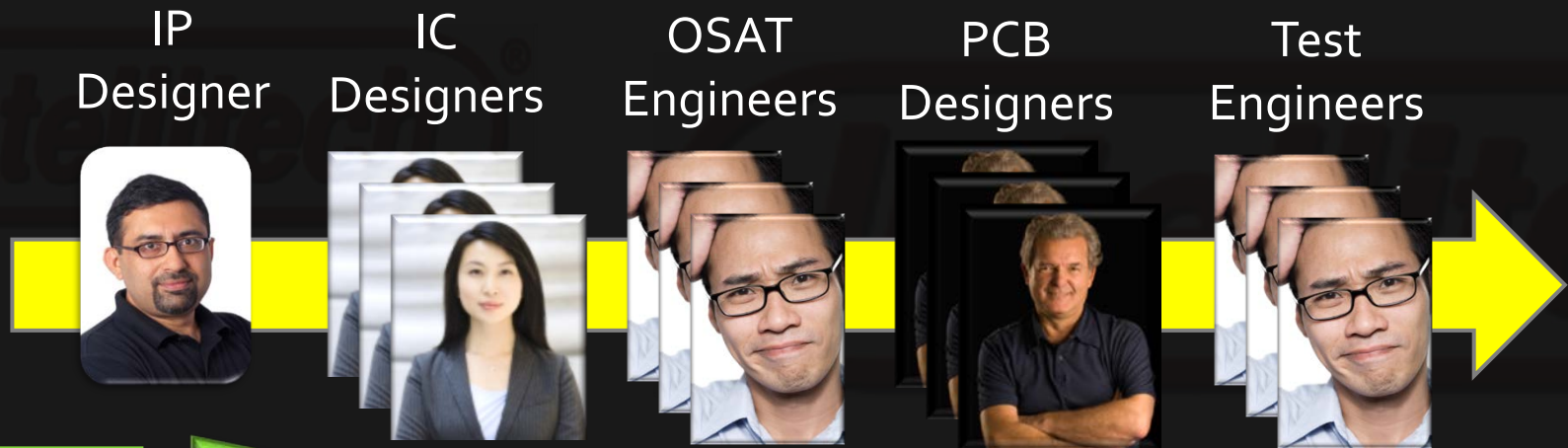


# 1149.1-2013 enables knowledge transfer

Through the standard hierarchical English-like languages of 1149.1-2013, IP and IC designers can transfer critical expertise to customers

One 1149.1-2013 compliant IP gets leveraged across hundreds of engineers

One 1149.1-2013 compliant IC may have hundreds or thousands of IP



**IP Domain  
Expertise**

Closest  
to source

Furthest

OSAT = Out Sourced Assembly & Test

**Total Industry  
Cost Savings**

\$

# Infrastructure Intellectual Property Vendor



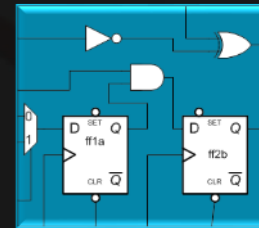
I make infrastructure IP.

How do I ...

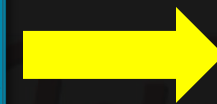
- Make it compatible with other Infrastructure IP?
- Document it so my customer can use it ?
- Minimize support and exonerate my IP when integrated into the customer's IC?

Ex. SERDES PRBS

Verilog description is not enough  
CTL vectors are non-retargetable



IP



IC  
Customer





# IC Designer

## I need Infrastructure IP but...

- a) Documentation is incomplete or unclear
- b) Hundreds of IP - I need automation
- c) How do I exonerate my chip when EMS has a board test problem?
- d) How do I reduce support but enable my customers to do complex ecosystem tests (e.g. test from IC to DDR3 at-speed)?



IEEE 1149.1-2013 & IEEE 1500 for IJTAG

# System Designer

I need on-chip and ecosystem tests

I want to characterize signal integrity of PCB FR4  
before software has functional tests

Datasheet isn't enough info

How do I run this on-chip IP?

How do I get EMS/Board test up  
to speed quickly?



# EMS Test Engineer and OSAT Test Engineer

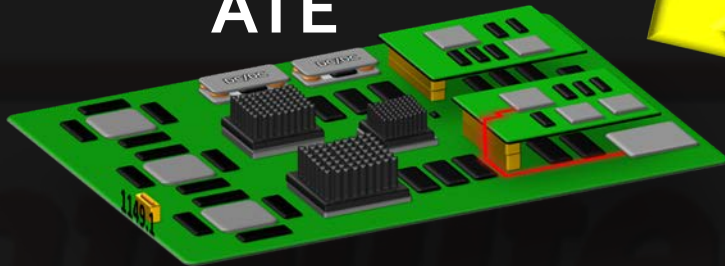


- I have many customers with different IP and different technology, I can't be an expert in all of them
- Test specifications have grown exponentially
- I need a scale-able automated approach

TEST  
SPECIFICATIONS



Board  
ATE

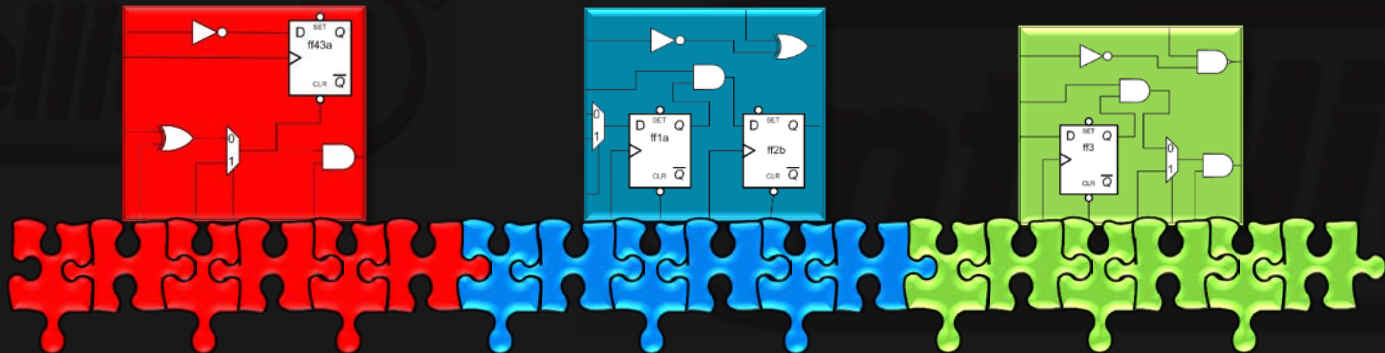


IC ATE

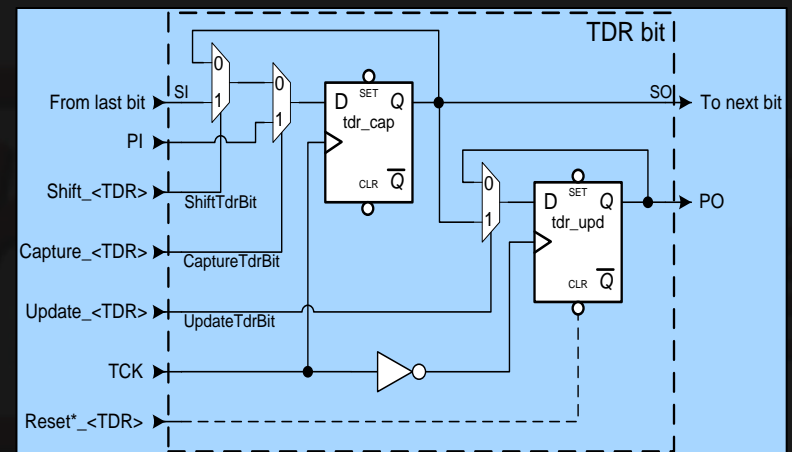


# Solution 1149.1-2013 - Make IP interfaces plug-n-play

- Standardized Test Data Register interface
- Standard defined cell types
- Each cell plugs into the next cell
- Plug-n-play interface

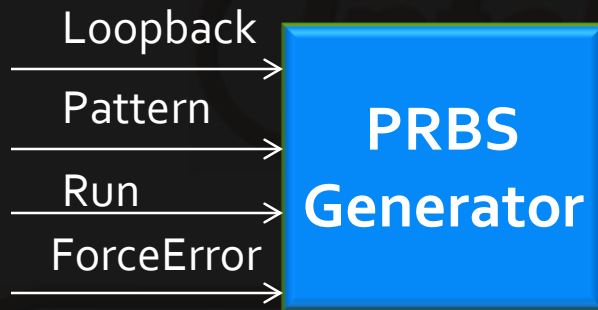


- Follows IEEE 1500 standard Wrapper Serial Ports
- Pre-defined Cell types
- User defined cells allowed



**Single bit TDR Cell**

## 1149.1-2013 Solution: Standardize IP documentation



- Describe Interface to IP w/o TAP
- Description is "packaged" in compliant IEEE 1149.1-2013 package file
- Describe just interface + mnemonics
- Machine readable

```

Attribute REGISTER_MNEMONICS of SERPRBS : package is
"OnGroup      (ON (1), OFF (0)), " &
"PatGroup     ( PRBS31(1), PRBS23 (2), PRBS7(3) );"
  
```

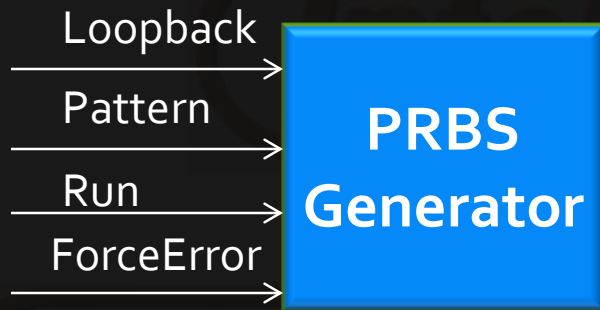
**Attribute REGISTER\_FIELDS of SERPRBS : package is**

```

"PRBS [5] ( "&
"(Loopback   [1] IS (4) DEFAULT(OnGroup(ON)), " &
"(Pattern    [2] IS (3,2)  DEFAULT(PatGroup(PRBS7)) ), " &
"(Run        [1] IS (1)    SAFE(OnGroup(OFF)) ), " &
"(ForceError [1] IS (0)) DEFAULT(OnGroup(OFF));"
  
```

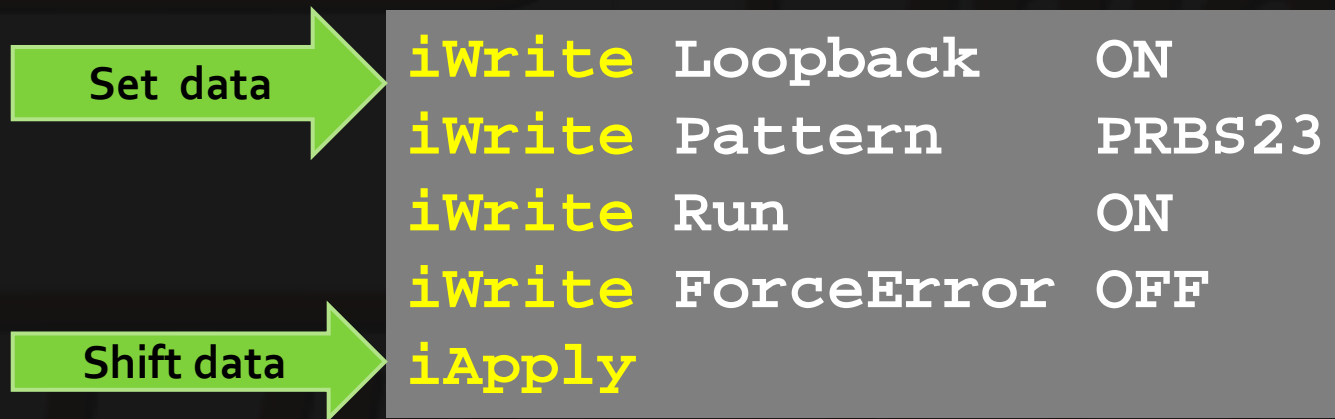
**PRBS - Pseudo-Random Bitstream Sequence**

# 1149.1-2013 Solution: Standardize IP documentation



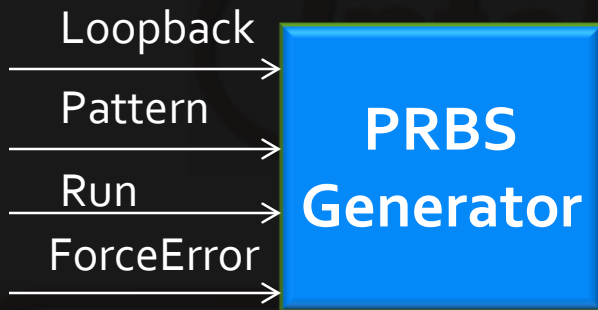
## Procedural Description Language

- new vectorless re-targetable language for describing IP operation



Format: **<iWrite >** <Register> <value or mnemonic>

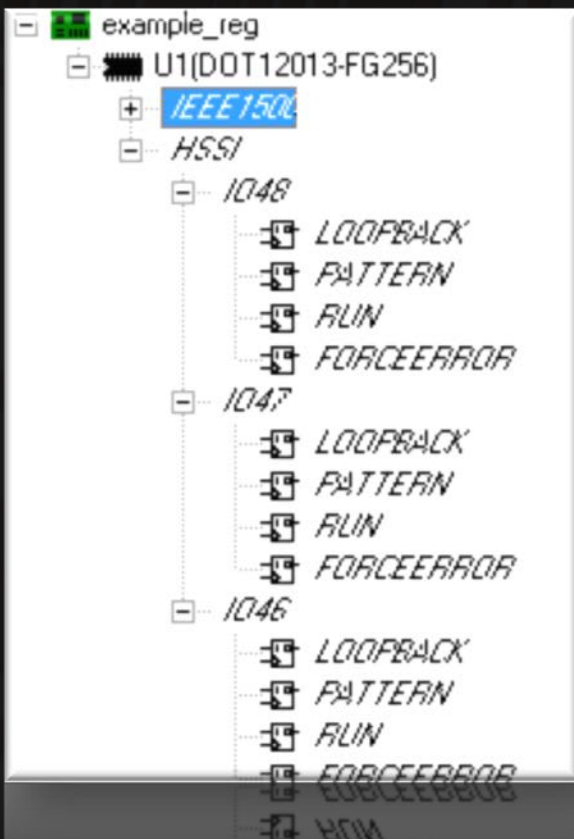
# 1149.1-2013 Solution: Standardize IP documentation



Tools read IP package file hierarchy  
And integrate with top level IC

1149.1-2013 <info tag> specifically provided  
for interactive operation of internal JTAG  
registers

Any instance of any IP can be accessed  
within the IC hierarchy



Screenshot of a table showing the configuration for EXAMPLE\_REG.U1.IO48. The table has columns: Pin, Name, Radix, To UUT, From UUT, and Expected. The table is currently set to OFF.

Pin	Name	Radix	To UUT	From UUT	Expected
	U1 . INSTRUCTION (4)	M	SERDES	0100	0001
	LOOPBACK (1)	M	OFF	X	X
	PATTERN (2)	M	PRBS23	XX	XX
	RUN (1)	M	OFF	X	X
	FORCEERROR (1)	M	ON	X	X

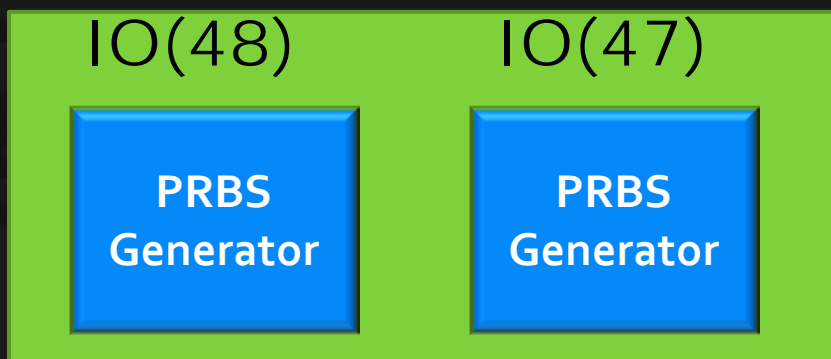


# Tools re-target register access for the user



Package SERPRBS

**iWrite** Loopback ON



HSSI

Package SERPRBS  
Package HSSI

Tool converts to: **iWrite** HSSI.IO(48).Loopback 1



Package SERPRBS  
Package HSSI  
IC BSDL

Tool converts to: **iWrite** U1.HSSI.IO(48).Loopback 1

# 1149.1-2013 Solution: Standardize IP documentation

## Memory BIST example "IP package"

**attribute REGISTER\_MNEMONICS of MEMB : package is**

```
"Mode (chkbrd      (0B000) <Checkerboard>, "&
"   GalPat      (0B010) <GALPAT >, " &
"   MATS+      (0B101) < March Algorithm >, "&
"   MOVI       (0B110) < Moving Invert >, "&
"   March_C-   (0B111) < Unlinked CFins >), "&
"Run  (Start     (1), " &
"     Stop      (0) ), " &
"Result (Pass    (0B11), " &
"       Fail    (0B01), " &
"       Not_Done (0BX0))";
```

Algorithm

Command

Status

Memory  
BIST

**attribute REGISTER\_FIELDS of MEMB : package is**

```
"MBist [6]( "&
" ( Algorithm[3] IS (5 DOWNT0 3) DEFAULT(Mode (Walk1)) NOUPD ), "&
" ( Command  [1] IS (2)          DEFAULT(Run  (Stop )) ), "&
" ( Status   [2] IS (1 DOWNT0 0) CAPTURES(Result(Pass )) ) );
```

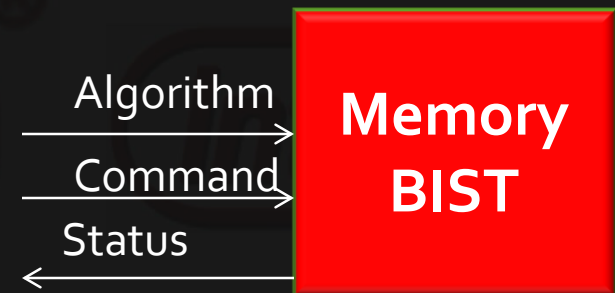
**BIST = Built-in Self Test**

## 1149.1-2013 Solution: Standardize IP documentation

PDL Description of how to operate MemoryBIST IP  
Memory\_bist procedure takes Algorithm and clock source

```
# MEMB.pdl
iPDLLevel 0 -version STD_1149_1_2013
iProcGroup MEMB
iProc memory_bist {alg clk} {

    iWrite Algorithm $alg
    iWrite Command Start
    iApply
    iRunLoop 10000 -sck $clk
    iRead Status Pass
    iApply }
```



"Without 1149.1 based I/O initialization, it could take a whole month on the IC ATE to configure the I/O for parametric testing on a complex SoC using functional test methods "

- IC Test Engineer  
Major OEM Company

(It's no easier at the board level!)

# 1149.1-2013 Solution: I/O parameters on new "init\_data" TDR

```

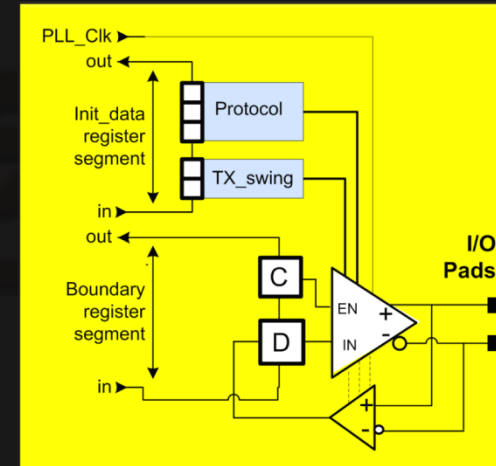
package body MyCorp_SERDES is
  use STD_1149_1_2013.all;

  attribute REGISTER_MNEMONICS of MyCorp_SERDES : package is
    "SerDes_Protocol ( "&
    "  off  (0b000) <Powered down>,"&
    "  SATA (0b010) <Serial Adv. Technology Attachment>,"&
    "  SRIO (0b011) <Serial RapidIO>,"&
    "  XAUI (0b101) <10Gbps Attachment Unit Interface>,"&
    "  Resvd1 (0b100) <Reserved for Future Use> , ),"&

    "SerDes_TX_Outputs ( "&
    "  off          (0b00) <Powered down> , "&
    "  Full_Swing   (0b01) <100% Vdd Swing> , "&
    "  75%_Swing    (0b10) <75% Vdd Swing> , "&
    "  52.7%_Swing (0b11) < Not valid for XAUI>)"&

  attribute REGISTER_FIELDS of MyCorp_SERDES : package is
    "Channel [5] ( "&
    "(Protocol [3] IS (2,0,1) SAFE (SerDes_Protocol(*))), "&
    "(TX_Swing [2] IS (3,4) SAFE (SerDes_TX_Outputs(*))) "&
    " ); "
  end MyCorp_SERDES;

```



## 1149.1-2013 Solution: I/O parameters on new "init\_data" TDR

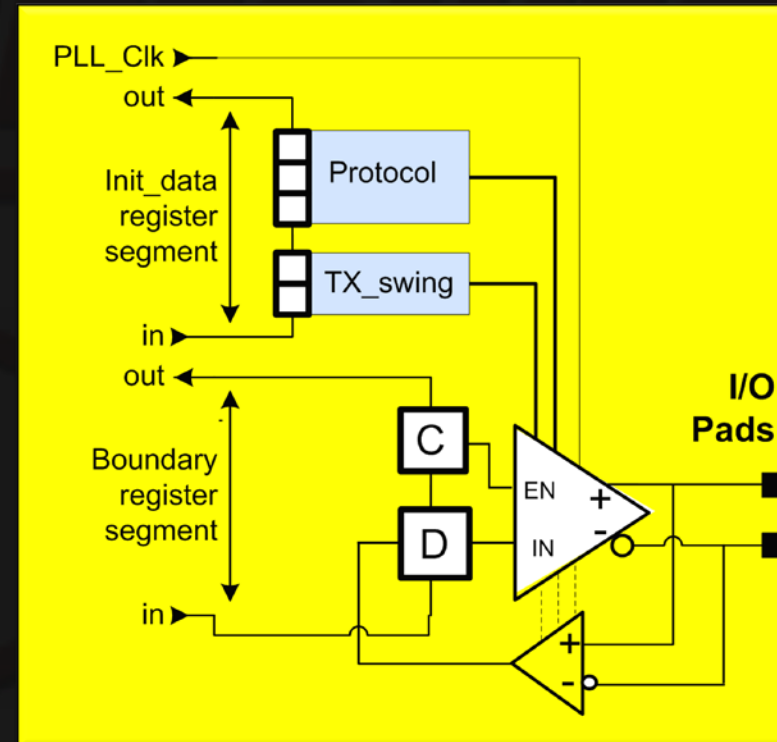
```

# MyCorp_SERDES.pdl
iPDLLevel 0 -version STD_1149_1_2013
iProcGroup MyCorp_SERDES

iProc init_setup {} {

    iWrite Protocol XAUI
    iWrite TX_Swing 75%_Swing
    iApply
}

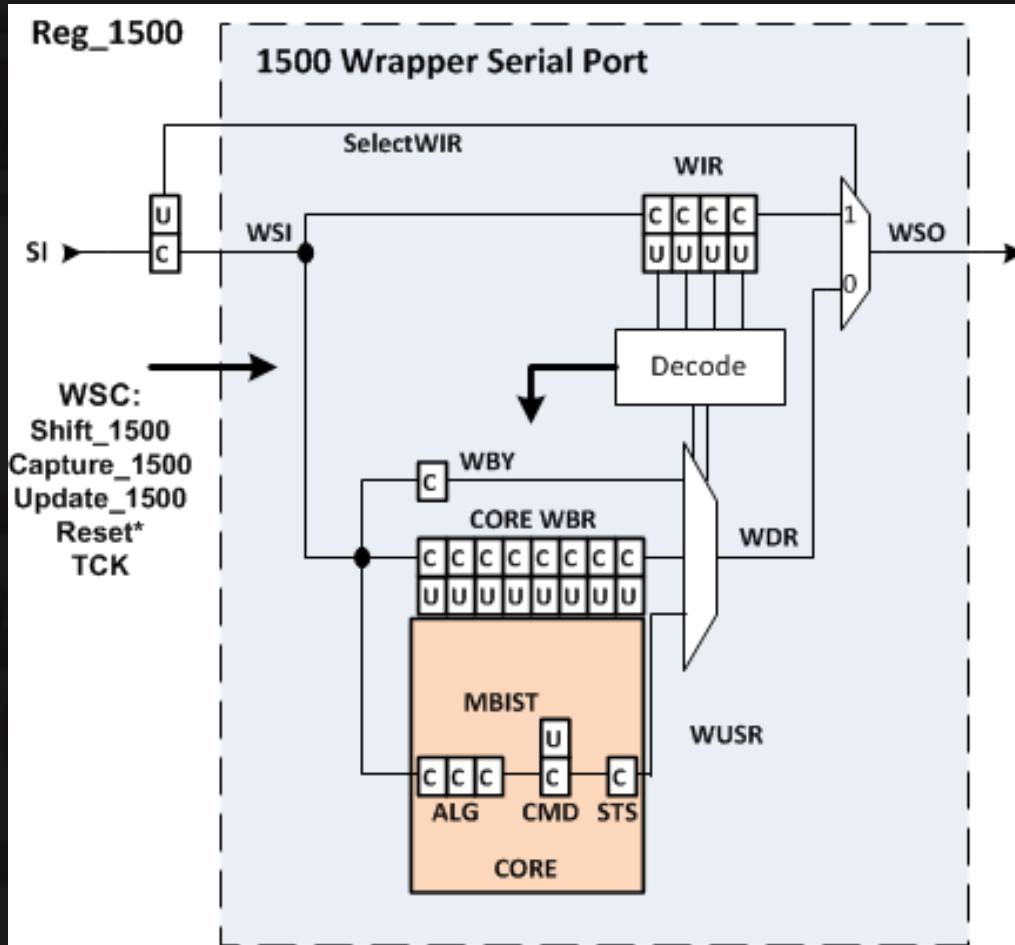
```



# IEEE 1149.1-2013 and IEEE 1500

- IEEE 1500 provides internal JTAG access
- Together: Powerful synergy for testing complex SoCs
- This combination the foundation of P1838 3D-SIC

CORE with 1500 Wrapper and MBIST (See prior description)



Can be described by 1149.1-2013 Package File Syntax

# IEEE 1149.1-2013 and IEEE 1500

## Concise Description of 1500 architecture and WIR mnemonics

This 1500 architecture provides access to **MBIST** from vendor "EDA\_ABC"

Attribute REGISTER\_MNEMONICS of REG\_1500 : package is

```
"WIR_decode ( "&
  "WS_BYPASS (0B0000) <Wrapper Bypass Instruction>, "&
  "WS_EXTTEST (0B0001) <Wrapper Extern Boundary Instr>, "&
  "WS_INTTEST (0B0010) <Wrapper Intern Boundary Instr>, "&
  "WS_BIST (0B0100) <BIST Instruction>, "&
  "WP_ALL (0B1xxx) <Wrapper Parallel instructions> "&
  " )" & -- end of WIR_decode
  " );"; -- end of REGISTER_MNEMONICS
```

Attribute REGISTER\_ASSEMBLY of REG\_1500 : package IS

```
-- The Select WIR bit and the Wrapper Serial Port
"REG_1500 ( " & -- Reset to WBY
  "(SELWIR [1] DelayPO ResetVal(0b0) TAPReset ), "&
  "(WSP IS WSP_MUX) ), "& -- end of REG_1500
  "WSP_MUX ( "& -- The outer segments: WIR and WDR
    "(SelectMUX "&
      -- Reset to WBY
      "(WIR IS WIR_Seg), "&
      "(WDR IS WDR_MUX) "&
      "SelectField (SELWIR) "&
      "SelectValues ((WIR : 0b1) (WDR : 0b0)) ) ), "&
      -- end of SELECTMUX end of WSP_MUX
    "WIR_Seg ( (WIR_field [4] "&
      "ResetVal(WIR_decode(WS_BYPASS)) TAPReset)), "&
    "WDR_MUX ( "& -- The inner segs: WBY, WBR, and Wusr
      "(SelectMUX "&
        "(WBY IS Reg_WBY CAPTURES(0) ), "&
        "(WBR IS Reg_WBR), "&
        "(WUSR IS Package EDA_ABC: MBIST) "&
        "SelectField (WIR) "&
        "SelectValues ("&
          "(WBY : WS_BYPASS, WP_ALL) "&
          "(WBR : WS_EXTTEST, WS_INTTEST) "&
          "(WUSR : WS_BIST) "&
          " )" & -- end of SelectValues
        " )" & -- end of SelectMUX
      " ), "& -- end of WDR_MUX
    "REG_WBY ( (WBY[1] NOPO)), " &
    "REG_WBR ( (WBR[8] ))" &
  end REG_1500;
```

**EXAMPLE\_REG.U1.IEEE1500.MBIST**

Pin	Name	Radix	To UUT	From UUT	Expected
	U1.INSTRUCTION (4)	M	ENA_1500	0100	0001
	ALGORITHM (3)	M	CHKBRD	011	XXX
	COMMAND (1)	M	START	0	X
	STATUS (2)	M	00	NOT_DONE	XX

**EXAMPLE\_REG.U1.IEEE1500.WRAPPER**

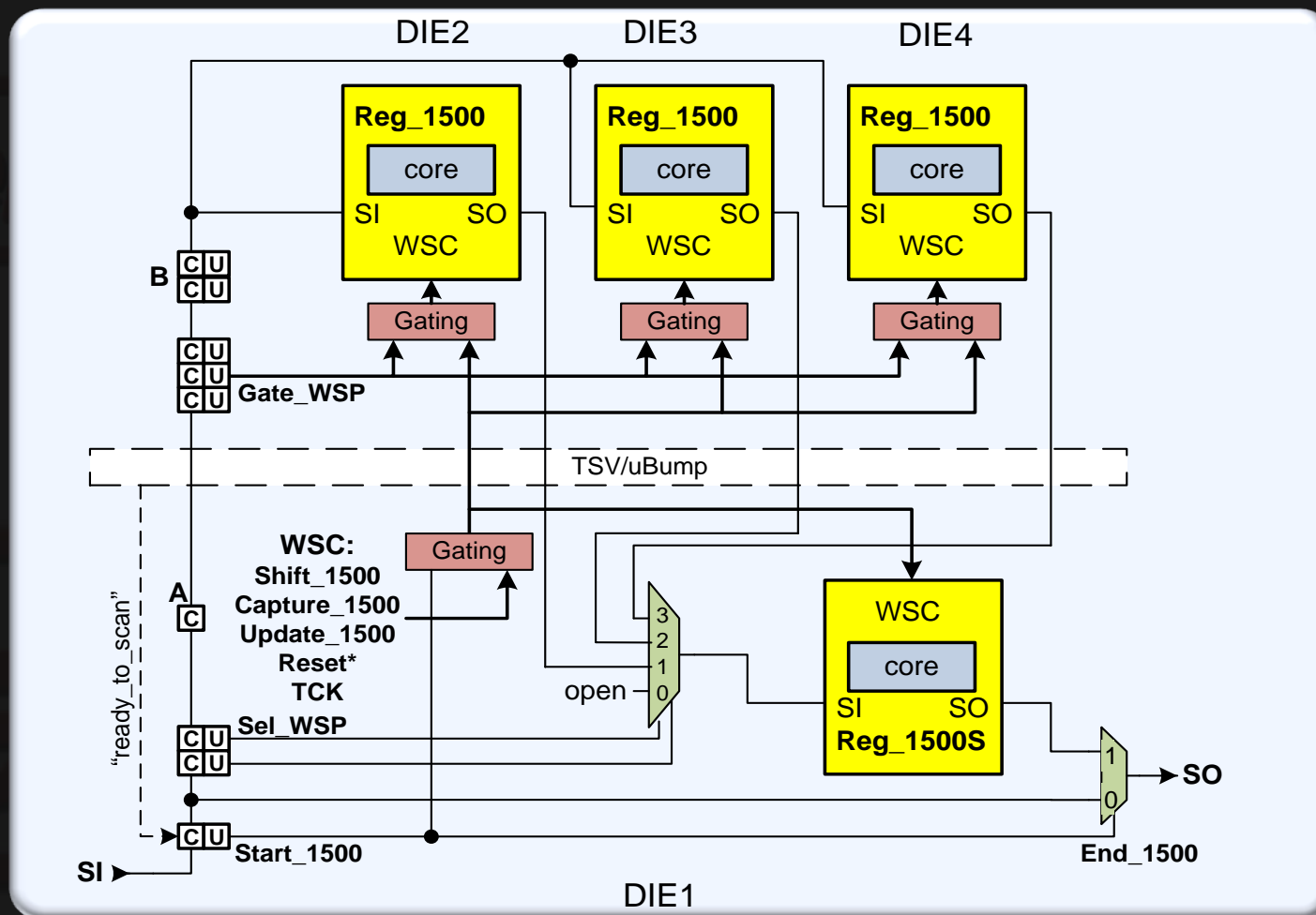
Pin	Name	Radix	To UUT	From UUT	Expected
	U1.INSTRUCTION (4)	M	ENA_1500	0100	0001
	WIR (4)	M		0100	XXXX
	WBR (490)	H	54A	3FE00C900	XXXXXXXXXX
	WBY (1)	B		0	X



# IEEE 1149.1-2013 and IEEE 1500

IEEE 1149.1-2013 expands IEEE 1500 Wrapper Serial Ports

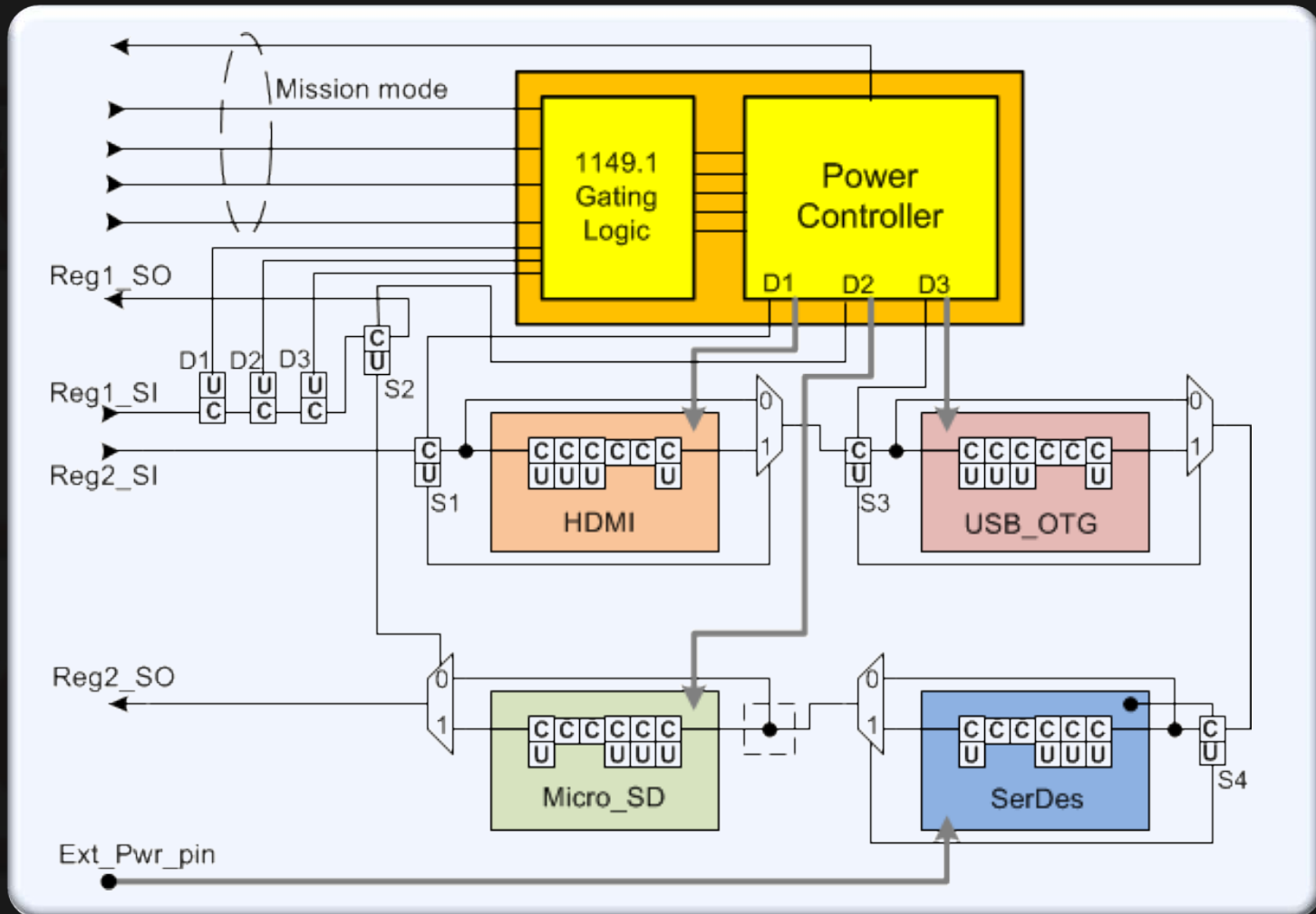
- Provides for standardized Domain/DIE crossing
- Attribute **REGISTER\_ASSOCIATION** enables TSV -to-register mapping
- Supports **BROADCAST** to IEEE 1500 WSPs



# IEEE 1149.1-2013 and IEEE 1801

Standardizes Test Data Register segmentation implemented by IEEE 1801 power intent. Both standards now use Tcl as the standard language.

Standardizes the input and description of on-chip or off-chip power control



## IEEE 1149.1-2013 New IC level Instructions

INIT\_SETUP  
INIT\_SETUP\_CLAMP  
INIT\_RUN

IC\_RESET

ECIDCODE

CLAMP\_HOLD  
CLAMP\_RELEASE  
TMP\_STATUS

Three Instructions for  
initializing programmable  
IP connected to I/O pins

Standardized on-chip per  
domain system reset

Unique per die identifier

Standardizes a method to  
hold and isolate I/O pins  
during in-situ test of an IC

**1149.1-2013 flexibility allows for any design power/speed/complexity  
but 1149.1-2013 architecture and rules enable any customer to drive  
a compliant IC without re-training**

**IEEE 1149.1-2013 and IEEE 1500 help combat  
'anything goes' DFT creativity**



**Creativity: Good here**



**Not good here**

**- Cost savings occur when interfaces are familiar, consistent,  
repeatable and don't require new training or analysis**

"From a cost stand point, having one way to communicate to an on-chip IP that works, is far better than having 100 different ways to learn and exonerate on each IC"

- Director of Engineering  
Tier 1 Semiconductor Supplier

## **For 23 years IEEE 1149.1 compliance has been a requirement for many ASIC and SoC contracts**

**Purchase Orders from Silicon vendors for on-chip infrastructure IP will also include requirements for IEEE 1149.1-2013 compliance**

**SoC and ASICs will include more external ecosystem test operated via 1149.1-2013**

**OEM Purchase Orders will include requirements for 1149.1-2013 compliance and IP with compliant documentation. OEM's will require the 1149.1- 2013 features for test.**



**The 1149.1 brand continues To give assurances to Customers that IP and ICs Meet an acceptable Level of simplicity for Test Re-use**

# 1149.1-2013 - It's an evolution!

<http://grouper.ieee.org/groups/1149/1>

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