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Intellitech iJTAGServer leverages Cadence Incisive Enterprise Simulator for IEEE 1149.1-2013 Silicon Instrument verification

Interoperability enables pre-silicon verification of IP blocks and comprehensive metrics on documentation and operational quality

Dover, NH --(October 5th, 2015) - Intellitech® Corporation, the technology leader in solutions for IEEE 1149.1-2013 Silicon Instrument™ development, has announced interoperability between its NEBULA silicon debugger, iJTAGServer and Cadence® Incisive® Enterprise Simulator. The iJTAGServer acts as a bridge linking Intellitech's open standards based silicon debugger with Incisive Enterprise Simulator. The solution enables IP developers to create IEEE 1149.1 compliant documentation of "Silicon Instruments" - JTAG accessible IP blocks - and get validation metrics on the documentation and code quality via Incisive pre-silicon. The pre-validated documentation can then meet the System-on-Chip (SoC) integrator's requirements for IP blocks that use IEEE 1500 style wrappers connected to the IEEE 1149.1 Test Access Port.

The Intellitech NEBULA software reads IEEE 1149.1-2013 compliant models which describe the instrument registers and wrappers abstractly. This enables the use of IEEE 1149.1-2013 Procedural Description Language (PDL) to perform transactions to and from the Silicon Instrument registers in simulation via the iJTAGServer software bridge to Incisive Enterprise Simulator; as would be done post-silicon in a real SoC. IEEE 1149.1-2013 PDL is used as a complement to SystemVerilog for verification, where it has specific capabilities targeted for 1149.1/JTAG style serially accessible silicon instruments. For instance, PDL enables tools to manage the internal scan access to the Silicon Instrument through IEEE 1500 wrapper serial ports and scan segmentation due to power-domains. Such access is cumbersome and time consuming to achieve in SystemVerilog. Once PDL for a silicon instrument is validated pre-silicon, it never needs to be modified again. It can be used by the SoC integrator, the IC ATE engineer and the PCB designer - throughout the life-cycle of the SoC - without conversion to vectors. PDL can be used directly on major IC ATE using another Intellitech bridging product.

"Verification with code coverage metrics via Incisive Enterprise Simulator is a key element to our mutual customer's first silicon success," said Patrick Dutrow, senior marketing manager with the Cadence Connections Program. "Intellitech's iJTAGServer bridge allows customers the ability to use the IEEE 1149.1/JTAG standard descriptions directly with Incisive Enterprise Simulator for comprehensive verification that provides a significant time-to-market advantage", he added.

"Debug of third party IP on ATE has consistently been a bottleneck to productivity. We see the IEEE 1149.1-2013 standard as a critical specification for efficient use of third party IP. The Intellitech toolset provides us with a methodology to link to simulation for pre-silicon validation of the IP and our ASICs", said Mike Fung, ASIC Test and Characterization Manager at Teradyne. "Having a common source for the verification environment and the test environment accelerates test debug an order of magnitude faster compared to traditional methods", Mr Fung continued.

"In the past, JTAG accessible IP blocks were delivered with an IEEE 1500 wrapper, some incomplete documentation and some test vectors with long strings of binary ones and zeros" said CJ Clark, Intellitech's Chief Executive Officer (CEO). "Typically the patterns wouldn't work on the IC ATE once reformatted and flattened for the SoC, causing an impact at a critical time in the SoC schedule. One customer tells me that, two years ago, it took them two months of back-and-forth with the memory controller IP provider to get patterns working during first-silicon bring-up. The IP was a black box, with no ability for the customer to understand or adjust simple controller parameters via JTAG. Today, with IEEE 1149.1-2013 PDL, Intellitech's iJTAGServer and Cadence Incisive Enterprise Simulator, the same customer was able to pre-validate the IEEE 1149.1-2013 descriptions in simulation and this time the memory controller IP bring-up took just four days", Clark concluded.

About Cadence Connections Program

The Cadence Connections program promotes interoperability in all areas of electronic design, bringing value and third-party solutions to customers' design chain. Connections Program members develop integrated software solutions that extend and add value to Cadence's leading design and verification technology. With more than 130 member companies, the Connections program has the industry's largest collection of third-party solutions working together with Cadence to make our mutual customers more successful. Information about the Connections program may be found at www.cadence.com/partners/connections/

About Intellitech Corporation

Intellitech is the technology leader in solutions based on IEEE 1149.x related standards. The company is sought out by customers to provide methodologies, IP and tools which lower a customer's cost in developing or manufacturing an electronic product. More information about Intellitech can be found at www.intellitech.com. Intellitech is a registered trademark of Intellitech Corp. in the U.S., E.U. and other countries. Silicon Instruments is a trademark of Intellitech Corp. Information about Intellitech can be found at http://www.intellitech.com

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