# IEEE 1149.10-2017 Tutorial


CJ Clark

Intellitech, CEO

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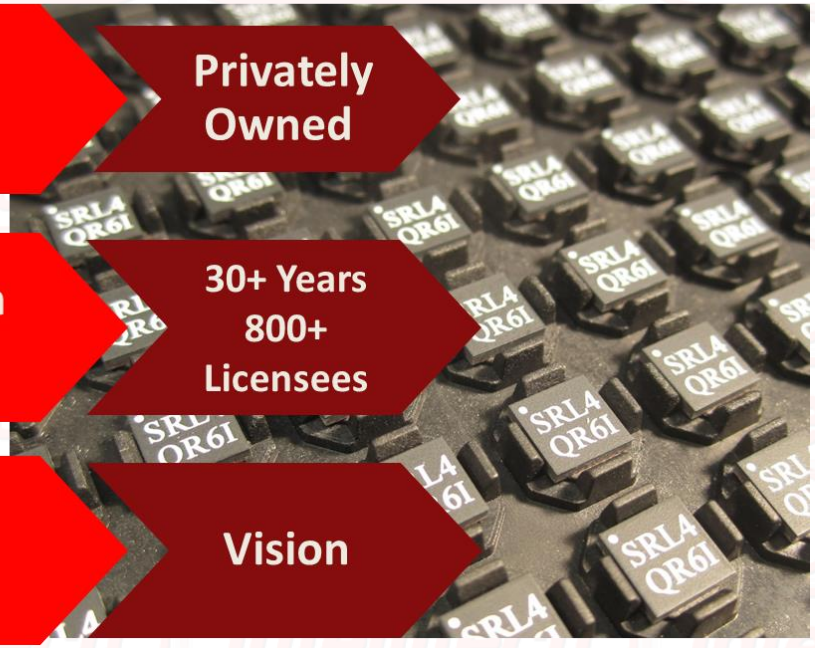
- IEEE Standards Medallion recipient for "*Vision, leadership and exceptional dedication in enabling IEEE standards to lower costs for the electronics industry*".
- Elected IEEE 1149.1-2013/JTAG chairperson
- Elected IEEE 1149.10-2017 chair/editor
- He is co-inventor on seven US with foreign counterparts related to JTAG and FPGAs.

# About Intellitech Corporation | IEEE 1149.x Solutions

Leading supplier of IEEE 1149.x based ATE & Software

| | | |
|---|---|---|
| Well Established | Headquarters in Rochester, NH & Fujisawa, Japan | Privately Owned |
| Proven | Stable long-term investors | 30+ Years 800+ Licensees |
| Expertise | Respected IEEE Standards Contributors | Vision |



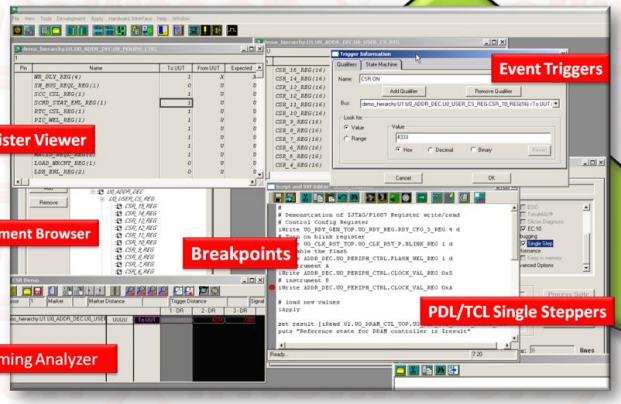
# Intellitech - What we do

**Board/System ATE & JTAG Controllers**

**Silicon Instrument IP, Patents & Services**

*Seven US Patents With foreign counterparts*

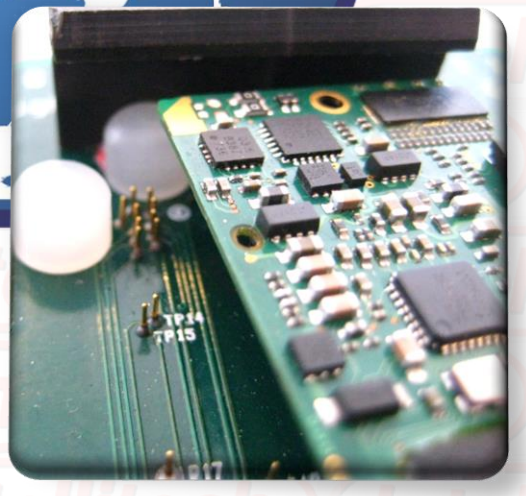
**1149.X TEST DEBUG CONFIGURATION**




**Silicon Instrument Verification & Debug Software**


**System Test and Configuration ICs**

# Intellitech customer locations



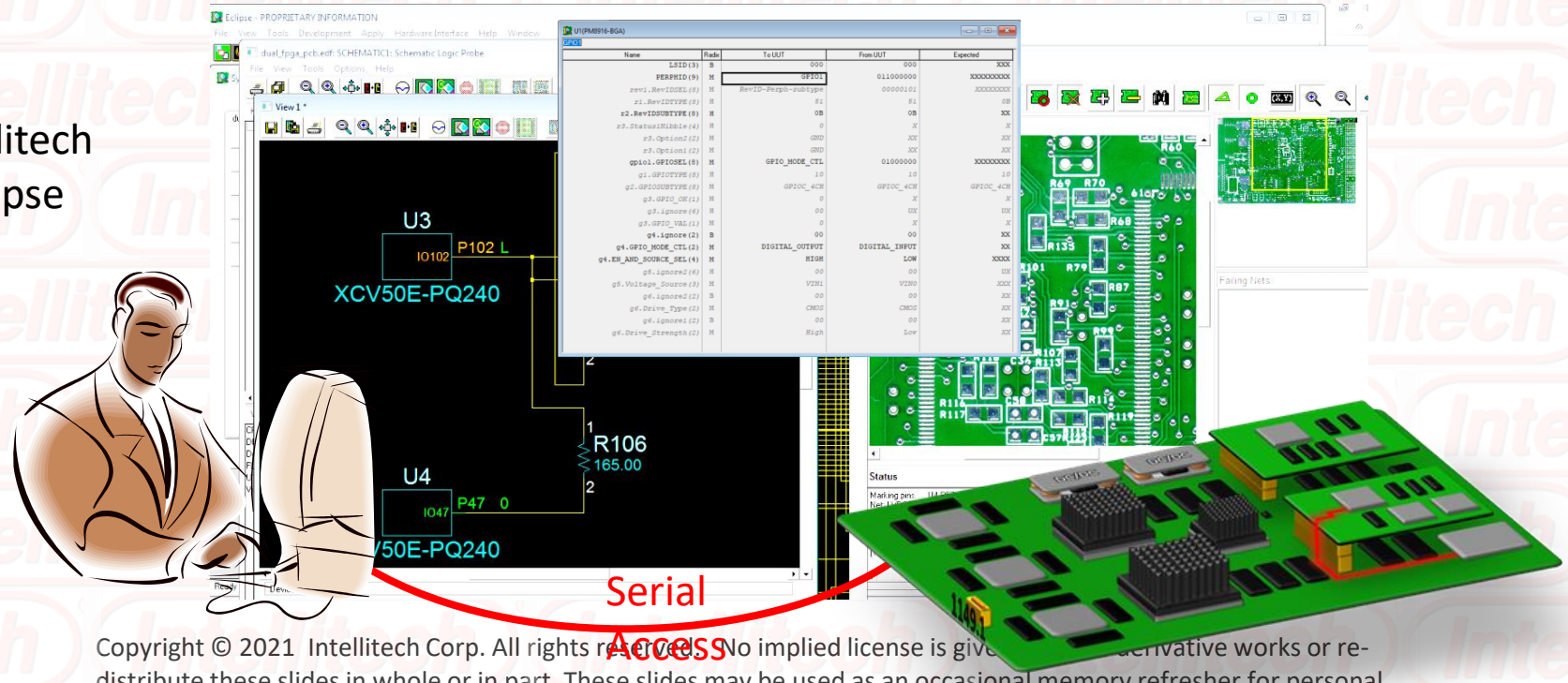
# Intellitech's software is like a web browser for an IC, PCB or System

Google Chrome or Microsoft Edge Browser

Serial Access

WWW World Wide-Web

Intellitech Eclipse




Serial Access

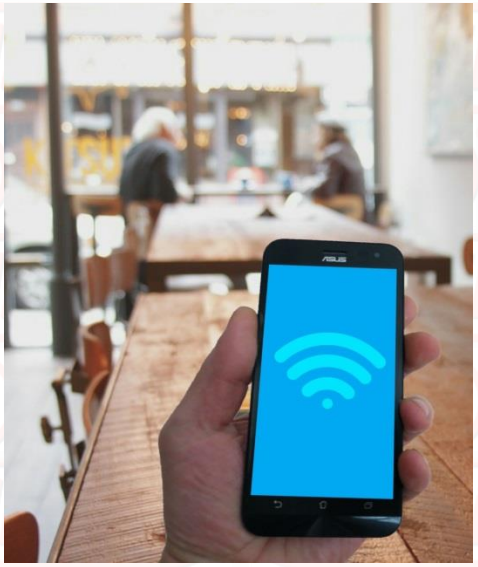
# Do you specify Wifi for components and devices?

**Do you specify**

- **IEEE 802.11g-2003**

**or**

- **IEEE 802.11ax-2021**



**Why give customers ICs that conform to IEEE 1149.1-2001 when what they need is IEEE 1149.1-2013?**

# IEEE 1149.1-2013 (JTAG)

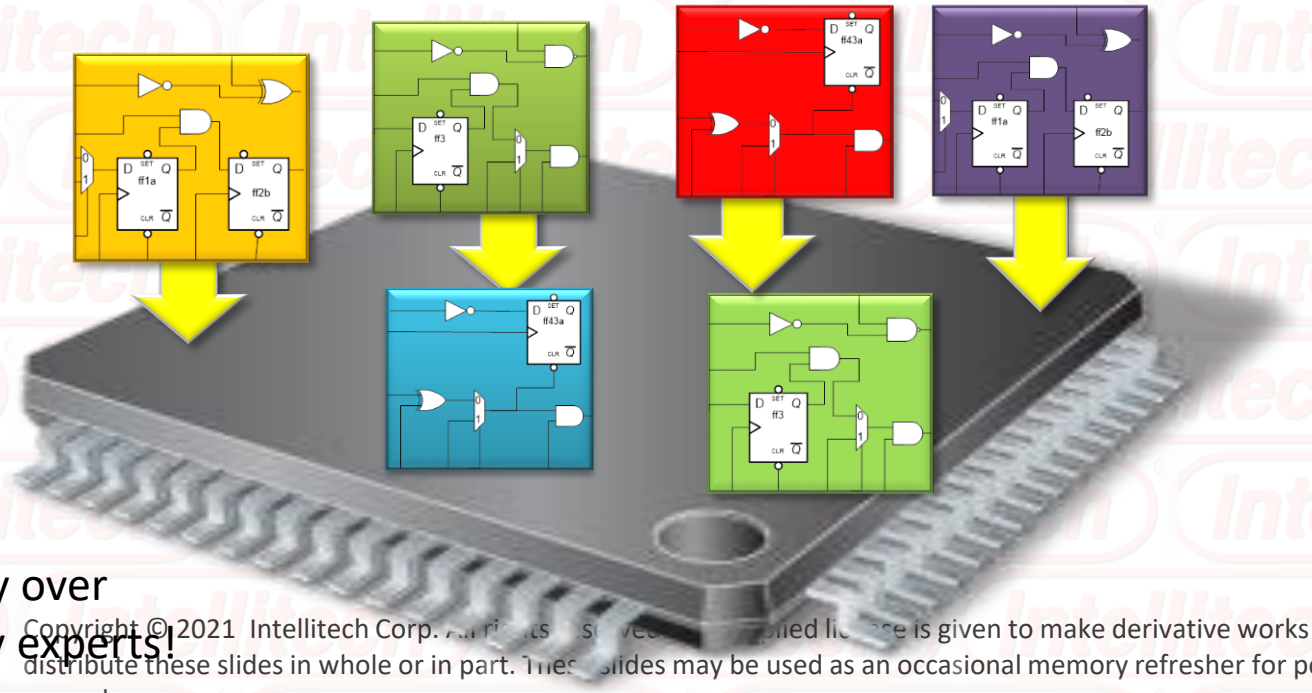
- Standardizes a plug-n-play test interface to IP blocks in an IC
- Standardizes a hierarchical structural language for the IP registers
- -Standardizes a procedural operation language (PDL) based on Tcl/TK

**Silicon Instruments™ = IP blocks**

**Memory BISR**
**SerDes BIST**
**PVT monitors**
**Ext. DDR BIST**
**PLL Control**
**JTAG2AXI drivers**

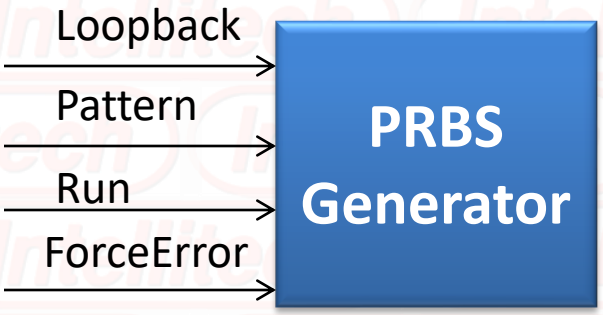
**Mission IP**

**GPIO**
**ADC**
**DAC**
**Connectivity**
**Analog**
**Etc.**




Approved by over
120 industry experts!

# What does it look like?

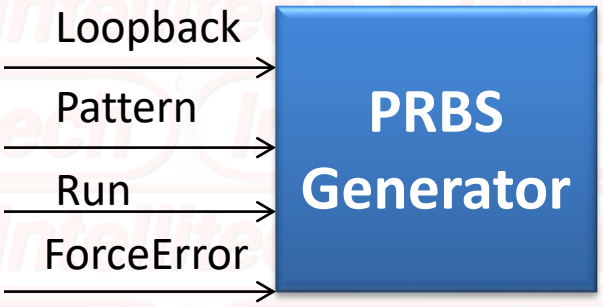



- Describe Interface to IP w/o TAP
- Description is "packaged" in compliant IEEE 1149.1-2013 package file
- Describe just interface + mnemonics
- Machine readable

```
Attribute REGISTER_MNEMONICS of SERPRBS : package is
 "OnGroup       (ON (1), OFF (0))," &
 "PatGroup     ( PRBS31(1), PRBS23 (2), PRBS7(3) )" ;

Attribute REGISTER_FIELDS of SERPRBS : package is
"PRBS [5] ( "&
  "(Loopback    [1] IS (4) DEFAULT(OnGroup(ON))), " &
  "(Pattern      [2] IS (3,2)  DEFAULT(PatGroup(PRBS7)) ), " &
  "(Run          [1] IS (1)     SAFE(OnGroup(OFF)) ), " &
  "(ForceError [1] IS (0)) DEFAULT(OnGroup(OFF)))" ;
```

# 1149.1-2013 Solution: Standardize the IP documentation




**PDL = Procedural Description Language**

- **new vectorless re-targetable language for describing IP operation**
- **Hierarchical (Self-contained for the IP)**

Set data

Shift data

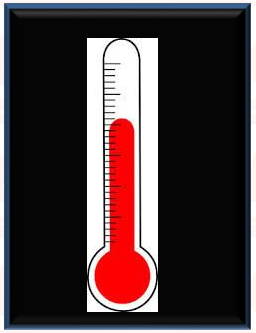
```
iWrite  Loopback    ON
iWrite  Pattern     PRBS23
iWrite  Run         ON
iRead   Result      PASS
iApply
```

**Format: <iWrite > <Register> <value or mnemonic>**

# Register documentation alone is not enough!

- **Customer wants pre-engineered solution**
  - **Instrument and software plug ‘n play**
  - **Need robust language (math operations, logical operations, etc) needed to make sense of data scanned out**

Temp Monitor



$$Voltage = 10 \times \frac{\kappa T}{q} \times \ln(10)$$

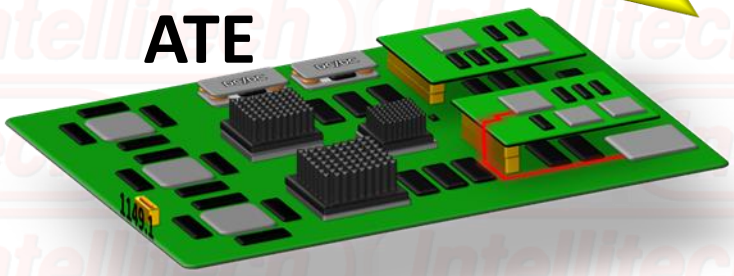
**IEEE 1149.1-2013 PDL required!**

```
iProc read {} {
set reg [iGet tempregister]
set temp =  ([$reg x 503.975]  / 4096) - 273.15
return $temp
}
```

# Why standardize documentation?

- **No time to read 1000 page PDFs**
- **No time to learn/build tools around different formats of a dozen IC suppliers**
- **SoC customers need scale-able automation**
- **Can't be an expert in all technologies**
- **PDF specifications have errors/ambiguities**
- **Need single format to Use @ silicon debug, wafer test, customer PCB bring-up, customer PCB test, etc.**

**Board ATE**



**SPECIFICATIONS**


**IC ATE**

Vendor B
PDF files +
Examples +
Program NVRAM

Vendor C
RISC-V
C++ Tools
+ PDF

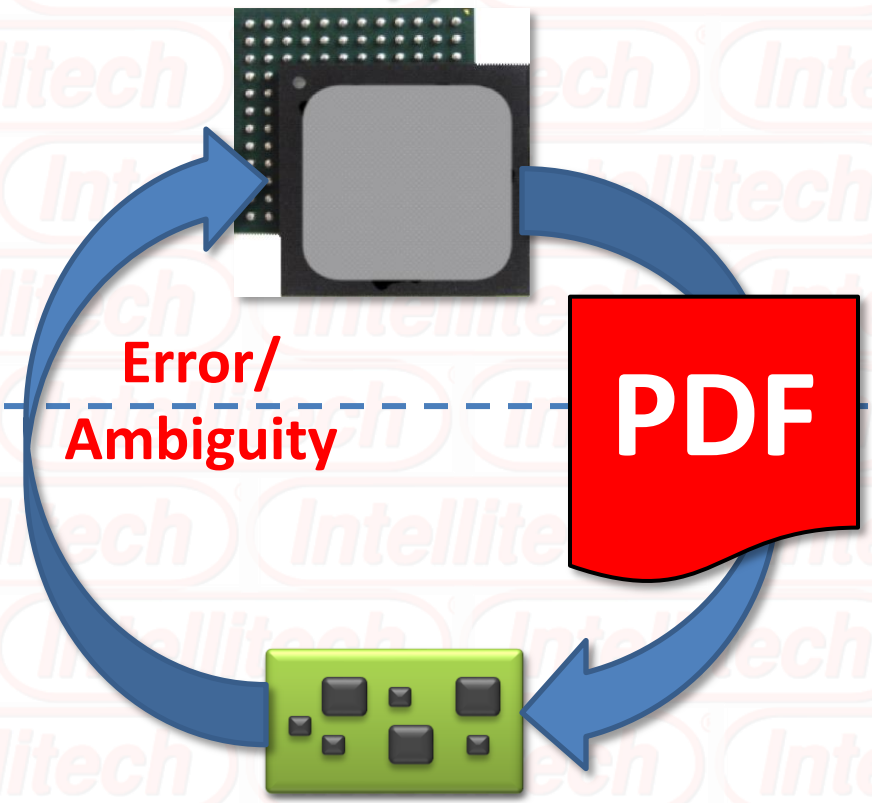
Vendor D
Evaluation PCB
with GUI App, program
NVRAM algorithm
+ PDF

Vendor A
ARM C++
Toolchain,
+ PDF +
Custom flash
programming

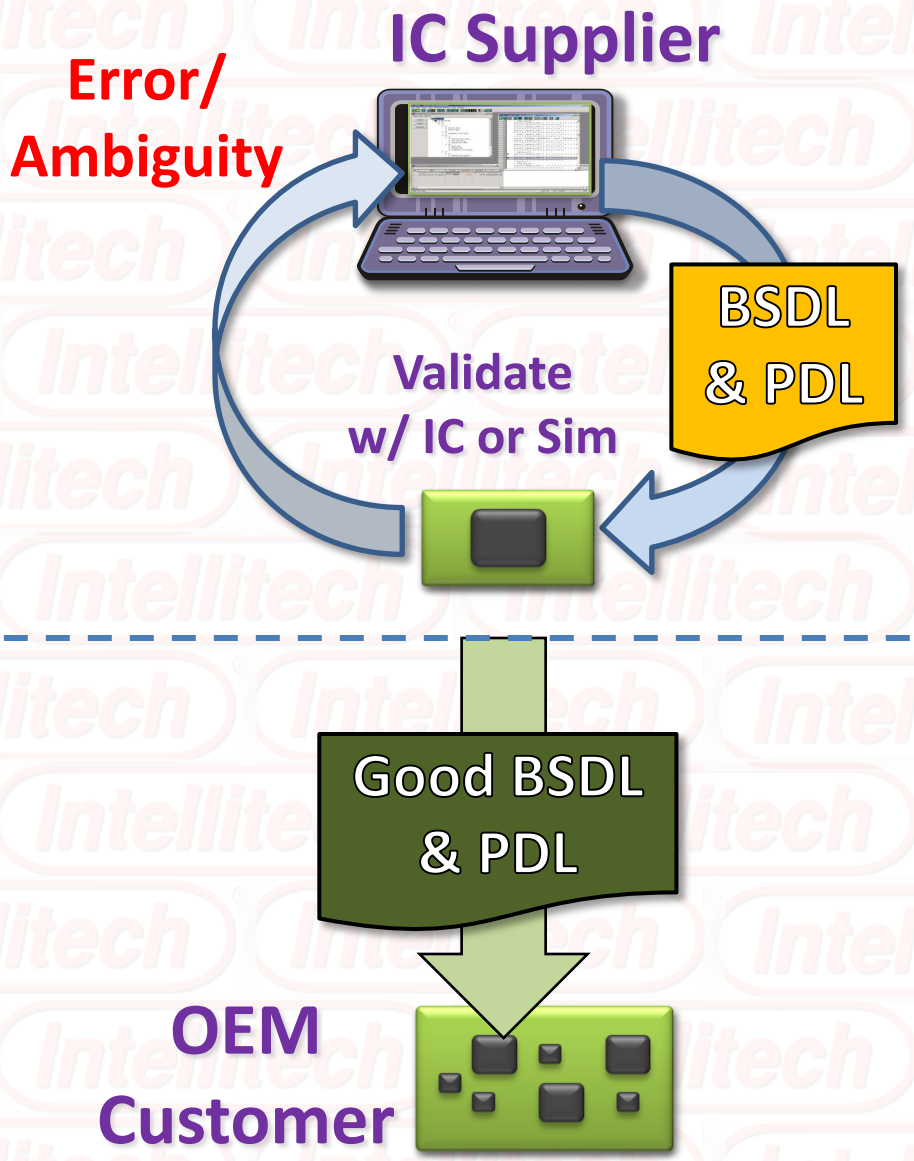
Vendor E
PDF Files
+ Proprietary
STIL patterns

Vendor F
PDF Files
+ VCD + XML

# PDF Documentation




# Standards Documentation



# What customers are saying:

"Debug of third party IP on ATE has consistently been a bottleneck to productivity. **We see the IEEE 1149.1-2013 standard as a critical specification for efficient use of third party IP.** The Intellitech toolset provides us with a methodology to link to simulation for pre-silicon validation of the IP and our ASICs. Having a common source for the verification environment and the test environment accelerates test debug an order of magnitude faster compared to traditional methods."

**Mike Fung**
**ASIC Test and Characterization Manager**
**Teradyne**

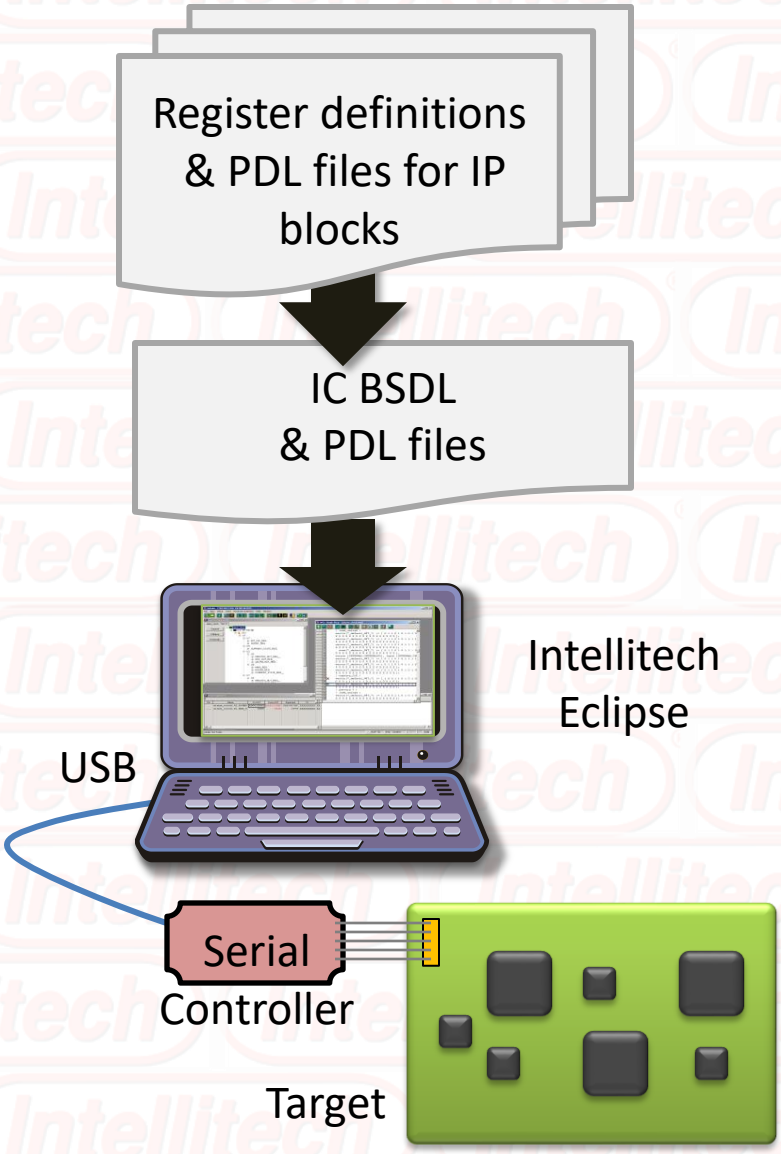
# What/Why IEEE 1149.10-2017?

*IEEE Standard for High-Speed Test Access Port and On-Chip Distribution Architecture – 80+ industry experts approved*

- Incorporate IEEE 1149.1-2013 by reference
  - Remove requirement for TAP
  - Remove requirement boundary register
  - Add support for SERDES packets
  - Add synchronous serial interfaces (SPI, I2C, SPMI, etc)

What's the motivation?

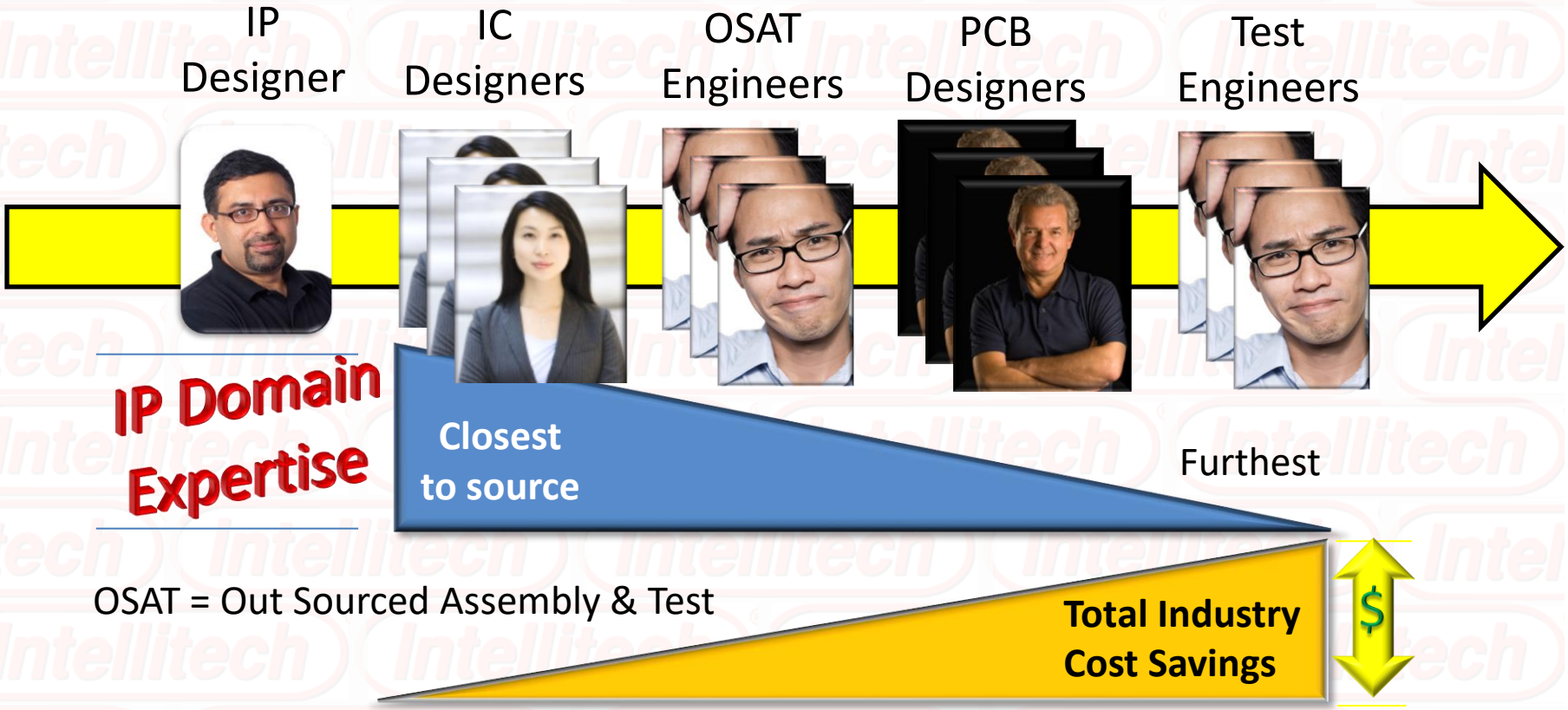
- Not all ICs have JTAG pins
- Many ICs and SoCs have non-digital pins
- Reduce IC design requirement.
  a. Mission mode interface has access!

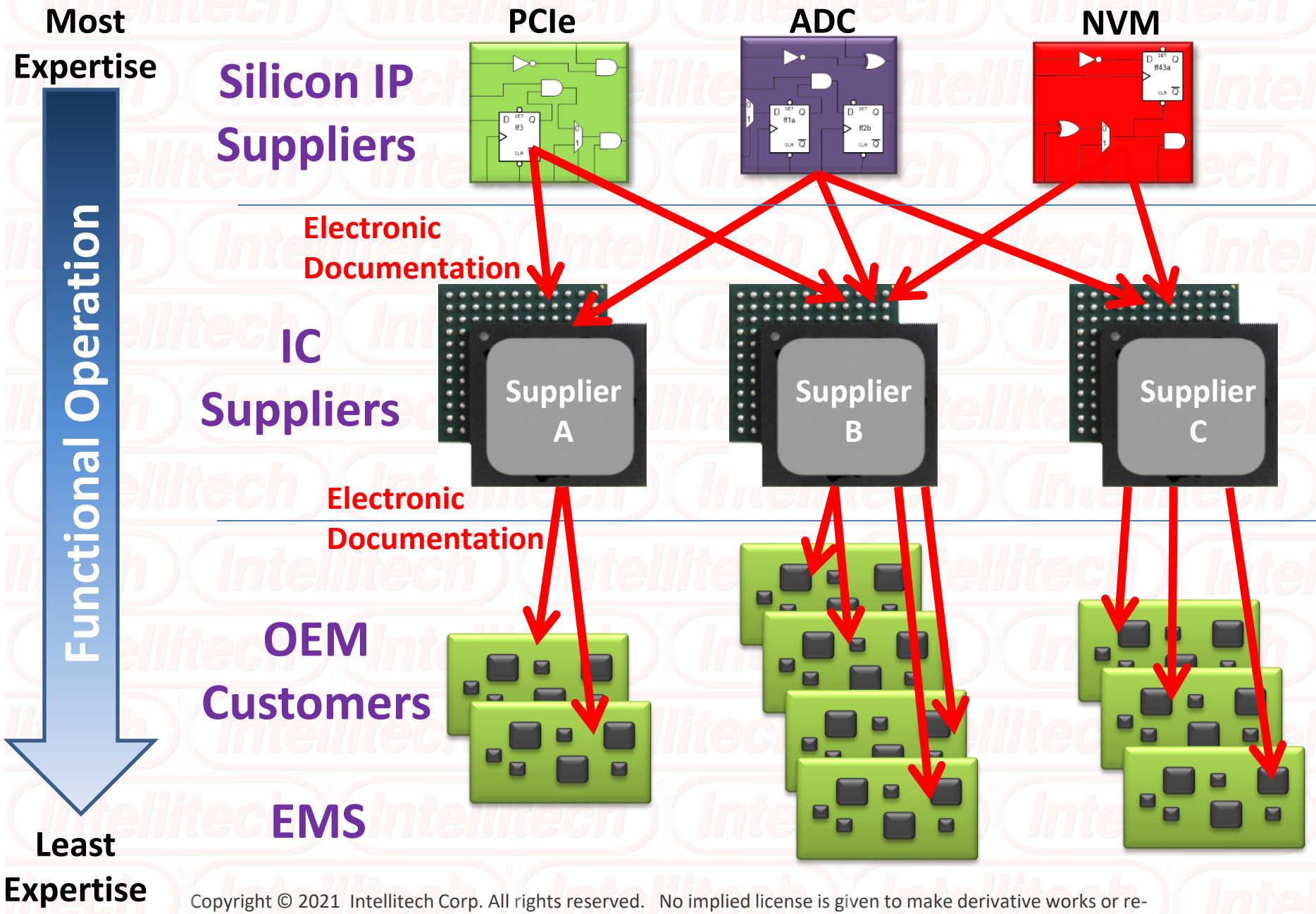


# Standards enable more reliable information transfer

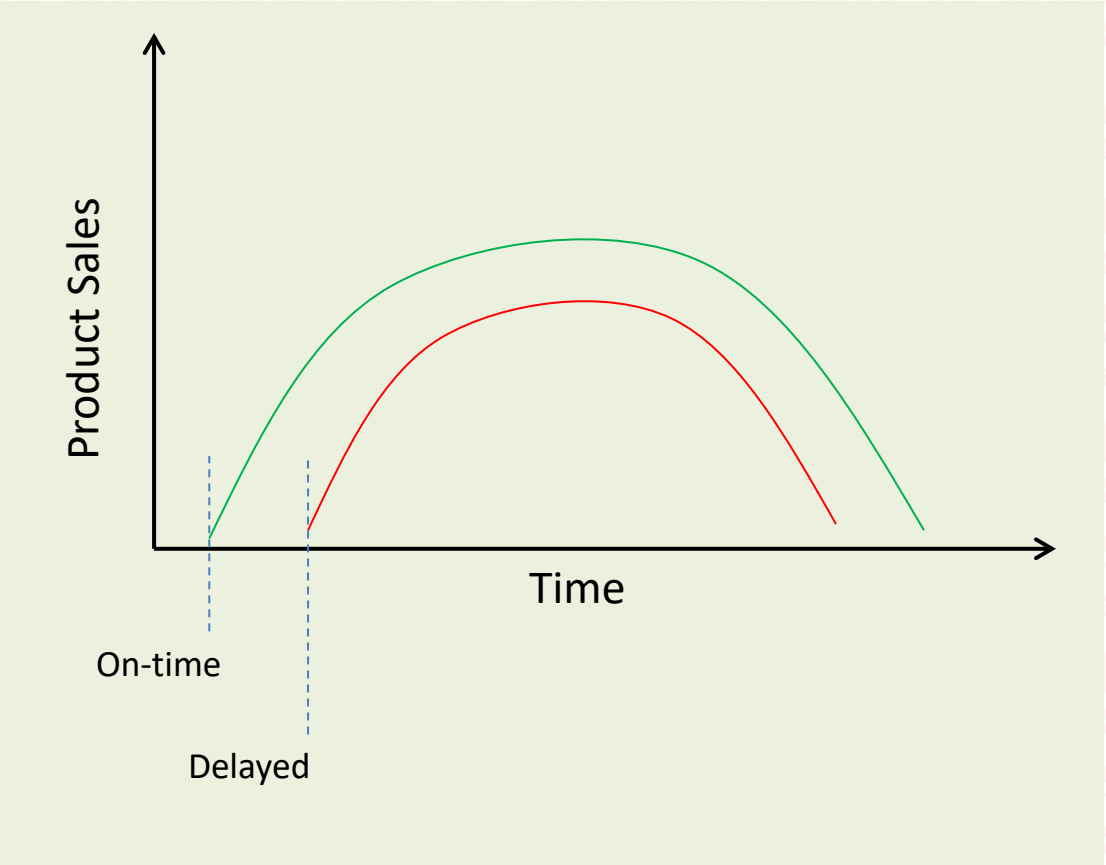
## IP and IC designers can transfer critical expertise to customers

One 1149.x compliant IP gets leveraged across hundreds of engineers
One 1149.x compliant IC may have hundreds or thousands of IP





IC Supplier and OEM customer both benefit from electronic documentation
Delayed entry due to documentation “challenges” affects OEM customer
Product revenue.  But also affects OEM customer IC purchase volume



# Compile and Go!