New Strategies for cost effective production PCB test and configuration

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About Intellitech

Intellitech's TEST-IP™ family provides patented and patent-pending infrastructure IP that enables customers to lower the cost of designing, debugging, producing and maintaining electronic systems. Intellitech's proprietary solutions enable customers to build self-testable and in-the-field re-configurable products with the least amount of engineering resources and at the lowest cost. Intellitech lowers production costs by embedding test or enabling parallel test of electronic assemblies during production test and burn-in. The unified test and configuration approach enables customers to lower manufacturing test costs, provide field adaptable products and retard product obsolescence with field upgrade-able logic.

The TEST-IP Intellectual Property is coupled with the Eclipse Scan-Based Diagnostic and Test tools to provide a powerful combination software-hardware tools for automatic test pattern generation, debug, and validation prior to embedding test and configuration data into the customer's product or passing to the PT100 production tester.

Intellitech Corp. is focused on providing a complete customer solution early during the design phase that ensures success. The engineering and support team is dedicated only to providing a comprehensive low cost configuration and test strategy for the entire product. Over the years, the company has been successful in being the first-to-market and driving major technology changes in IEEE 1149.1 based configuration, debug and test. Intellitech's PT100 Parallel Tester received the prestigious Test and Measurement World Editor's Best-in-Test 2004 award.

Intellitech's customer base ranges from companies providing the latest networking products to ATE companies providing cutting edge semiconductor testers, from semiconductor manufacturers to space related companies providing satellites to large computer companies delivering multi-processor systems. The company's broad product selection, strong support team, and compelling value proposition have resulted in solid profitability and a strong balance sheet. Intellitech has sales and support offices located in Durham, NH, Mountain View, CA, Ottawa, Canada, and Munich, Germany.

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Introduction

Test and configuration times for modern PCBs continue to rise while there is a need for production cycle times (sometimes referred to as the production 'beat rate') to decrease. As test and configuration times of complex systems continue to increase, there is a need for new strategies that can prevent the duplication of capital equipment in order to satisfy production volumes. Many of the current approaches to configuration and test are being challenged to keep up with the increasing complexity and cost constraints of today's boards and systems. Figure 1 shows the traditional In-Circuit Test (ICT) focused flow. This method encompasses FLASH programming either at ICT or, as shown, with off-board or in-line FLASH programming in order to achieve reasonable throughput in the line.

Figure 1. Traditional In-Circuit Focused Flow

This is followed by Automatic X-Ray Inspection (AXI), Automatic Optical Inspection (AOI), In-Circuit Test (ICT) with a bed-of-nails fixture, followed by Functional Test. ICT has become an all-encompassing test method, incorporating analog tests, discrete digital device tests, boundary-scan tests, FLASH programming if not done off-line/in-line and boundary-scan in-system programming. In order to achieve this, the ICT is supplemented with add-on boundary-scan controllers, dedicated FLASH programming controllers or add-on equipment for in-system programming.

Stage:	AXI	AOI	ICT	Functional
Total Test Time	30 sec	30 sec	Analog 10s Dis. Digital 10s CPLD Prog. 12s TestJet/Cap 8s Boundary-scan 40s Flash Prog. 73s Total 153s	30 sec
Testers:	1	1	4	1

Figure 2. Test times at each stage for a 40sec/PCB line rate

Each test stage along the line must be shorter in duration than the production cycle time. Conventional Test Engineer wisdom is to load more and more tests on to ICT to 'better utilize' the ICT and 'reduce handling'. However, adding more and more tests onto a single tester increases the total test time for that stage in the line. In Figure 2, the total ICT test time is 153 seconds, far exceeding the production line rate. It will require four ICT testers working in parallel to keep up with the line rate of 1 PCB every 40 seconds. The tests on the ICT include analog and passive tests,

discrete digital tests, CPLD programming, capacitive plate type tests such as TestJet, boundary-scan interconnect tests and FLASH programming. Looking at the total tests in the ICT stage, it is clear that adding the boundary-scan and FLASH programming onto the ICT caused the test time to increase from 38 seconds to over 153 seconds. Had FLASH programming and boundary-scan tests been done on another stage in the line, such as after ICT or during function tests, a single ICT would have sufficed for keeping up with the production line. As discussed in this paper, we will see that boundary-scan tests, CPLD programming and FLASH programming are all test and configuration methods that can now be tested in a highly parallel manner, much more efficiently than adding more ICT testers to the production line.

Figure 3. New flow based on PT100 Parallel Test

Innovative technologies are changing the production PCB test flow. Two important advances occurred in 2003 with the introduction of the Intellitech PT100 Parallel Tester at the International Test Conference in October. The PT100 introduced on-board programming of FLASH and other non-volatile memories at off-board speeds and parallel test over standard IEEE 1149.1 'boundary-scan' or "JTAG". The PT100 has one U.S. patented granted, and two other patents applied for in the US and worldwide pending. The PT100 performs test and on-board programming of as many PCBs as needed to keep up with the production line cycle time or 'beat rate'. The tester is expandable, needing less than US$1500 per UUT to be tested or programmed in parallel, all controlled by a single computer console with an available PCI or PXI slot.

Figure 3 shows the new flow based on PT100 parallel test. The flow eliminates the FLASH programming step and reduces the test complexity of the ICT to simple analog and low technology device testing requiring as few as pogo-pins as possible. In some cases just a Manufacturing Defects Analyzer (MDA) or older ICT could perform this function. Boundary-Scan test, In-System Programming, FLASH programming and High-End digital test functions, especially those related to FPGAs are performed in parallel. Each test or configuration step has been optimized so the step can be accomplished within the production cycle time. The strategy is to break the tests down into separate test types, each test type to be performed by equipment optimized for that test type (digital tests separated from analog tests). A more in-depth description follows.

Figure 4. PT100 with custom test rack & fixture

Boundary-Scan on In-Circuit

In the early 1990's boundary-scan was seen as a way of reducing the pogo-pins on an in-circuit tester (ICT). Boundary-Scan was only thought of as 'virtual' pogo-pins designed into digital ICs. By 1999, the limitations of using ICT pin electronics to deliver boundary-scan serial data became apparent when FPGA and CPLD vendors adopted IEEE 1149.1 for on-board programming of their devices. The large amount of serial patterns exceeded ICT pin electronics memory, requiring multiple data loads adversely affecting test times. ICT vendors responded with add-on hardware options such as "Lightning" from Teradyne and "FlashISP" from Agilent. ICT vendors, seeing the success of dedicated boundary-scan vendors, also began integrating dedicated boundary-scan hardware with the ICT platforms, with the intention of saving a 'handling step' and integrating the boundary-scan diagnostics. However, as this article will attempt to illustrate, integrating boundary-scan test onto an ICT platform is not suitable for all product types. Integrating boundary-scan onto ICT may actually increase test costs. **Figure 5** shows the effective utilization of a 2500 pogo pin ICT. The ICT capital investment can be estimated as a cost per pin. A typical value may be $120 per pin for a full function ICT, therefore a 2500 pin tester would be approximately $300K. If this same tester is only used to test PCBs under 2000 pins, then the utilization would drop to 80% (2000/2500). If this were the case, essentially, the test department has 'overbought', using a more expensive tester to test products that could be tested with a lower cost tester without loss of test coverage. In this case the effective cost per pogo pin would go to $150 per pin some 25% more.

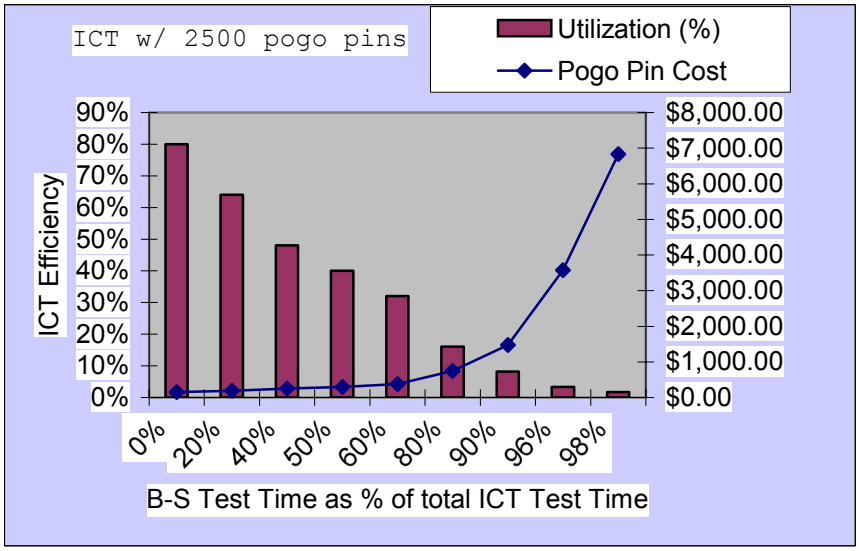

Figure 5

This same analysis can be done when combining boundary-scan test on ICT. ICT Test time is broken down into three major parts, Analog Test or "A", Digital Test or "D" and Boundary-Scan Test or "B". For this article "Digital Test" is being defined as the test of active digital components that can't be tested through boundary-scan. When boundary-scan tests are performed, only 4 pogo pins or dedicated boundary-scan controller is needed for boards designed with DFT (Design-for-Test) and boundary-scan in mind. Most of the ICT electronics other than the power-supply remains idle during boundary-scan test. As more time is spent performing boundary-scan tests, more of the time the ICT pin electronics are left idle. If the total ICT test time is 60 seconds, and half of that is

spent performing boundary-scan tests, then only 40% of the ICT resources (pin electronics, floor space, fixture, personnel, etc) are being used and the cost per pin shoots to roughly $3500 per pin. Performing boundary-scan tests on ICT in these cases is not an efficient use of the ICT resource. As boundary-scan test times increase, ICT utilization decreases when these separate test techniques are combined together. This also holds true for low volume product where flying-probe is used instead of ICT and a pre-built fixture. Adding long on-board programming or boundary-scan tests increases the cost of the flying probe time as the probe is held up waiting for the boundary-scan based test and configuration to complete.

Cisco test engineers report boundary-scan tests exceeding 3 minutes (240 seconds) or 98% of the ICT test time for a telecom type PCB. As seen in the graph, the ICT utilization would drop to less than 3%. Each time a PCB is tested in this case, only 3% of the ICT is being used. Using the ICT resources in this way is analogous to printing out an email letter and using a cargo plane to deliver it to the recipient in the next city. It's not very good use of the cargo plane that can carry more profitable heavy cargo. There is more effective equipment (computers) that can send the email, at a lower cost, even though the cargo plane *could* perform the task. In the same light, ICT *can* be used for boundary-scan test, however, it would be better use of the resource to use it for tests that require pogo-pins, backdriving, and analog test capability. **Figure** 6 shows a table of PCB types that could benefit from performing boundary-scan on ICT.

PCB Type	B-S on ICT?	Example
High BGA device and pin count Low analog/MSI component count	No	Telecom blade, DSP, Computer Blade
Panelized PCBs with FLASH/CPLDs	No	Automotive/Consumer/Appliance
PCBs with many digital plug-in modules	No	Motherboard/Workstation/Telecom
PCB w/ B-S Test < 2 x Analog + Digital Test time	Yes	Small industrial controller
High Analog content - 1 or 2 devices w/ b-s	Yes	Power Supply Controller

Figure 6

PCBs with small boundary-scan test times are suitable for integrating boundary-scan on ICT. If the boundary-scan test time is short, it wouldn't make sense to separate the boundary-scan test from the ICT. Anytime the boundary-scan test time, "B" is greater than twice the combined analog test time, "A" and Digital Test time "D", the tests should be separated as the boundary-scan tests could be tested in parallel with a parallel 1149.1 tester. Other factors should be considered as well such as how many circuits are on the PCB. Panelized PCBs with more than four circuits present a problem for integrated boundary-scan controllers on ICT. This is because there are typically only 1 to 4 boundary-scan interfaces that can be controlled by the dedicated controller. A PCB with '16 up' panels (16 like circuits on one PCB card) would have to be split into 4 sections of 4 circuits each to be accommodated by the ICT with dedicated boundary-scan controller. It is important to analyze for each PCB type, the fault coverage provided by boundary-scan, AXI and AOI, the test times and the FLASH programming needs before determining the test strategy.

Solder Joint	AXI	AOI	MDA or Simple ICT	B-S Only	Tested?
Digital SMT IC Input/Output pins		Yes	Some	Yes	Yes
Digital SMT IC Power/GND		Yes	Some	Some	Yes
Digital BGA IC Input/Output pins	Yes	No	No	Yes	Yes
Digital BGA IC Power/GND	Yes	No	No	Some	Yes
Series and Termination Resistors		Yes	Yes	Yes	Yes
Series Buffers/Voltage translators		Yes	Yes	Yes	Yes
Small Mixed signal IC(s)		Yes	Yes	No	Yes
Miscellaneous Passives		Yes	Yes	No	Yes
Bypass Capacitors		Yes	No	No	Yes
Edge or backplane connectors		Yes	Loopback	Loopback	Yes

Figure 7

Separating boundary-scan from ICT also does not affect test coverage. See **Figure 7.** Some test engineers may say that they need the test points to hold non-boundary-scan devices in a 'safe' state. This may be true for PCBs that do not have the proper DFT (Design-for-Test). However, tools from Intellitech will analyze a PCB netlist and identify these problem areas before the PCB goes to layout. If they still exist, then yes, what the test engineer is saying is that he needs test point access with a pogo-pin fixture, but not necessarily in-circuit tester pins. Costly, full-function in-circuit pin electronics are not needed to hold a chip enable or an output enable high or low. These PCB test points are held at a power or ground level for the duration of the boundary-scan test, which can easily be accomplished with the PT100 tester as well. The new PT100 production test flow uses ICT for what ICT does best, test analog and small discrete digital devices with full access. This can be done with a Manufacturing Defects Analyzer, which typically is one third the cost of a full fledge ICT, or with older depreciated ICT such as the GR227X or GR228X line. Yes, many of the older ICT have all that is needed for testing passive components, SSI/MSI digital devices and small mixed signal interface components still found on the most advanced PCBs. Ask any accountant and the most cost effective capital equipment is fully depreciated capital equipment!

Research by ICT vendors in the late '70s and early '80s indicated that digital ICs outputs could tolerate large current bursts for short periods (*i.e.* 'backdriving') without affecting the IC failure rate. This was instrumental in allowing ICT to gain acceptance in the industry without fear that ICs would be damaged by ICT techniques. However, this research and the design of most ICT pin electronics were done with 5V logic levels in mind. Recently, ICT vendors have been promoting their next generation architectures which will now test low voltage digital devices (LVTTL, 2.5V, 1.8V etc) 'safer'. With lower voltages, shorter 'backdriving' periods are needed with pin electronics that can automatically shut-off in shorter periods of time to prevent IC damage. It may appear that older ICT may not have much useful life. However, when the digital test on next generation PCBs is being shifted to the PT100, the older ICT will handle performing the limited analog, and MDA style tests. Only when ICT pin electronics require 'back-driving' (overdriving the output of a digital device with high-current, something that is never done with PT100 style boundary-scan tests) a low-voltage part would they require 'safer' tests, and even then, only in certain circumstances.

The PT100 parallel test strategy does not mean replacing ICT that is already owned, merely using this asset more efficiently. Much of the complexity on a modern motherboard, DSP board, telecom board that needs to be tested can be tested through boundary-scan. Customers report PCBs with

over 10,000 solder connections having only 800 solder connections that could not be tested in some way with boundary-scan. Half of those connections were due to digital bypass capacitors, which are best tested by AOI, not ICT. Test techniques such as AXI and AOI provide important coverage for BGA power and ground connections and miscellaneous passives.

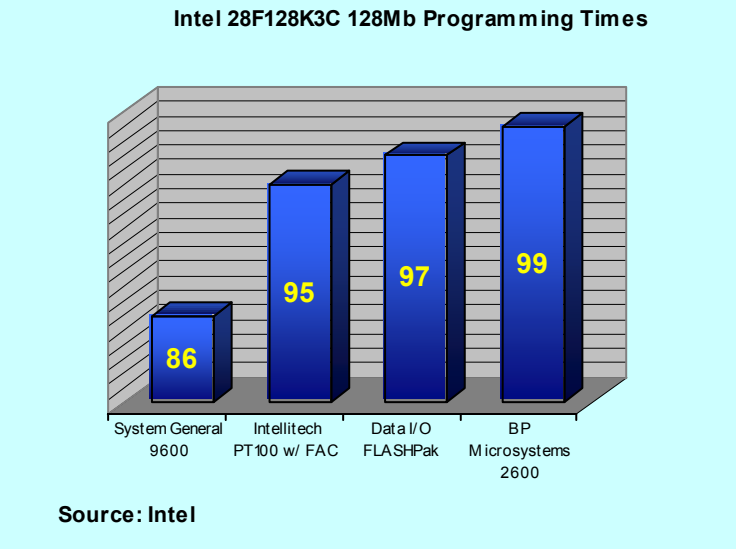

Figure 8. FLASH programming w/ PT100 comparison

FLASH Memory Programming

Programming FLASH memory and other non-volatile memories is an important part of the PCB assembly and test process. Modern PCB assemblies typically have one or more non-volatile memories that need to be configured prior to final test. In the early days of ICT, memories were small enough that they could be programmed on the ICT. However, today's non-volatile memories can take over a minute to program, which would exceed the production cycle time or 'beat rate'. Current methods to overcome long configuration times include off board programming and inline FLASH programming. Both have their drawbacks in cost and planning. Programming FLASH off-board, even when performed by a dedicated programming house, has hidden costs such as inventory management, volume forecasting and shrinkage. If you program too early you risk missing a last minute firmware change, program too few and production is held up until more programmed devices can be delivered. Program too many and you've increased the parts cost of the product by that amount.

Vendors such as BP Microsystems and Data I/O provide FLASH-programming equipment so devices can be programmed at time of assembly. These programmers can program multiple devices at a time and with enough of them even the largest FLASH devices can be programmed within the production cycle time or beat rate. In-line programmers such as Data I/O's 'roadrunner' will program 4 FLASH at a time and interface directly to your pick and place machine.

Up until now, programming FLASH through boundary-scan was too slow, typically taking 10 or 20 times longer to program than direct physical access. However, the PT100 incorporates Intellitech's patented fast-access-controller technology (U.S. Patent 6,594,802 other foreign patents pending, See *Patents* sidebar) enabling the PT100 to program FLASH devices on-board as fast (sometimes faster!) as off-board techniques. See Figure 8 for a comparison of programming times for the Intel 28F128K3.

***Patents* Sidebar**

Q: *I'm producing products outside the U.S., why should I care about patents in the U.S. or elsewhere?*

A: Most countries' Intellectual Property laws (U.S, Japan, EU, etc.) protect not only patented designs in a product but also processes used to make the product. Products manufactured outside of a country using a process patented within the country the product is destined for, would be infringing on the patent. This is designed such that merely having a product manufactured in a country where the patent doesn't exist cannot circumvent domestic patents. The OEM and related distributors would be liable for patent infringement and products could be prevented from entering the country where the patent is held. Presumably, once the manufacturer's customer is affected, the manufacturer would ultimately suffer economic loss as well.

Programming with the PT100 and FAC is competitive with off-line and in-line programmers. Programming Flash efficiently was an important goal for the PT100 as this enables the PT100 based production line to eliminate non-volatile programming equipment, saving the cost of not only the equipment, but the sockets, handling, maintenance agreements, management and personnel associated with non-volatile programming.

Cost comparison

By optimizing the test equipment and moving more tests and programming to be done in parallel with the PT100, significant costs in capital equipment can be achieved. An example of the traditional ICT focused production test equipment cost is shown in Figure 9 with the new PT100 based production test equipment cost for a customer's PCB. The PCB has one Intel 28F640W30, two Xilinx XC95288XV CPLDs needing in-system programming and a number of boundary-scan and non-boundary-scan devices. Since it takes about 67 seconds to program the 28F640W30 on the best equipment available, an in-line programmer was chosen with four sockets.

PCB w/ Intel 28F640W30, 2 X95288XV CPLDs and a production cycle time of 30 seconds

Line Cost	Inline Programmer	AXI	AOI	ICT	Parallel 1149.1	Functional	Total
Traditional ICT focused	$150K	$300K	$150K	$300K+$50K*	N/A	$75K	$1.025M
Fixturing/Sockets	$1500 x 4			$15K	N/A		$21K
Test/Programming Time	67s / 4 = 17s	< 30	<30	10A+4D+16B = 30s		60s / 2 = 30s	
				=			
PT100 Parallel Test and Configuration	N/A	$300K	$150K	$100K	$60K	$75K	$685K
Fixturing/Sockets	N/A			$5K	$5K		$10K
Test/Programming Time		< 30	<30	10A+4D = 14s	(67P+16B) / 4 = 20s	60s / 2 = 30s	
Capital Cost Savings	$156K			$260K	($65K)		$351K

*ICT with add-on boundary-scan hardware

Figure 9. – Equipment cost savings PCB 1

The resulting one device every 17 seconds would be fast enough to keep up with a beat rate of 30 seconds. Since the PCB needed boundary-scan test and in-system programming of the CPLDs, an ICT with integrated boundary-scan controller from a third party was chosen. The ICT test time can be broken down into 10 seconds for the analog portion, 4 seconds for the discrete digital test portion and 16 seconds for the boundary-scan portion (10A+4D+16B = 30seconds). It is interesting to note the ICT test time was equivalent to the production line rate. If the line needed to speed up to handle higher volumes of product, a second 'all-in-one' ICT with boundary-scan controller would need to be added at an additional cost of $365K. If after production was started, additional boundary-scan or other ICT tests were identified that needed to be added to improve quality, a second ICT with boundary-scan controller would need to be added to keep up with the production rate. The all-in-one ICT approach creates a non-scalable bottleneck. In contrast, the PT100 flow shows a capital equipment cost savings of $351K. The PT100 flow required just a low end ICT/MDA with only 400 pins available, for less than $100K, and a PT100 at a cost of $65K. The PT100 provided a combined programming and boundary-scan test of 83 seconds for four PCBs in parallel providing throughput well under the 30-second cycle time. Just eight slots of a single PT100 chassis were used to handle loading/unloading of the PCBs while other PCBs are tested and programmed in

parallel. With 14s test time on the ICT/MDA and 20s test time on the PT100, there is plenty of room to add additional tests or decrease the cycle time in either stage of testing ICT/MDA or PT100. With the new PT100 focused flow, if the production volume increased by 16% (a new cycle time of 25 seconds), there is no increase in capital equipment needed for the PT100 and the associated lower cost ICT/MDA. Additional boundary-scan tests, such as cluster tests or memory tests can be added after production begins, even if they add 40% *more* test time without changing the line or adding capital equipment. With the addition of another PT100 test channel (at $5K), a 80% increase in test or programming times could be handled. Distributing the test elements to the equipment that can best handle the type of test needed allowed more flexibility to scale when test times increased or production volume increases.

PCB 2

Panelized PCB with 8 circuits of Intel 28F128K3, 2 Xilinx X2S200, CPLD, SRAM and cycle time of 48s

Line Cost	Inline Programmer	AXI	AOI	ICT	Parallel 1149.1	Functional	Total
Traditional ICT focused	$150K x 4	$300K	$150K	($300K+$50K) x 2**	N/A	$75K	$1.825M
Fixturing/Sockets	$1500 x 16			$30K	N/A		$54K
Test/Programming Time	96s for 16 IC	<45s	<45s	15A+5D+35B = 45s		90s / 2 = 45s	
PT100 Parallel Test and Configuration	N/A	$300K	$150K	$100K	$80K***	$75K	$705K
Fixturing/Sockets				$5K	$7K		$12K
Test/Programming Time		< 45s	<45s	15A+5D	(96P+35B) / 3 = 43s	90s / 2 = 45s	
Capital Cost Savings	$624K			$625K	($87K)		$1.162K

**Panel Split prior to ICT as boundary-scan controller can only test 4 circuits at a time

*** 24 controllers for three 8 circuit PCBs

The second example is a panelized PCB with 8 identical circuits used in the automotive industry. The 128Mbit FLASH takes 96 seconds to program (all locations were not used) on stand-alone programming equipment. 4 In-line FLASH programmers from Data I/O were needed to produce 16 ICs every 96 seconds. The FLASH programming dictated the line rate, enabling one PCB to be assembled every 48 seconds. It is interesting to note that while FLASH programming vendors divide the programming time by the number of devices in parallel to achieve a per device programming time, this math doesn't work well with panelized PCBs since all the FLASH locations need to be populated before the PCB can make its way to the wave solder machine. The ICT test time for this PCB is 15 seconds for the analog tests, 5 seconds for the discrete digital devices and 35 seconds for the boundary-scan test and configuration. The total test time on the ICT is 45 seconds. The 3rd party boundary-scan controller on the ICT can only test on four boundary-scan circuits at a time. Because there are 8 circuits on the panel requiring boundary-scan test and configuration, this caused an extra step of splitting the PCBs in half prior to going to ICT. In addition, since the test time is one of these split PCBs is 45 seconds, a second ICT with boundary-scan controller was added in order to keep up with the line cycle time (there are now two smaller PCBs every 48 seconds appearing to the ICT).

Using the PT100 parallel test method, a significant reduction in capital is required to achieve better results. The PT100 parallel test method saves over a $1Million dollars in FLASH programming equipment and ICT tester cost. With just 24 controllers, the PT100 can test and configure three PCBs at a time with a throughput of 43 seconds per PCB. In the future, if the cycle time needed to be reduced by roughly 25%, another eight PT100 controllers could be purchased for roughly $24K and the throughput could increase to one PCB every 32 seconds.

Conclusions

The PT100 is a scalable method of test and configuration that can adapt any length programming time, test time or handling time to any production beat rate. Long test and configuration times are handled simply by testing more PCBs in parallel from a single test resource. Adding small low cost test cards to the PT100 chassis can test additional PCBs from a single computer console at a much lower cost than boundary-scan on ICT or stand-alone boundary-scan controllers. By separating out the long boundary-scan tests from ICT, the PT100 returns the efficiency of ICT for discrete digital and analog tests, reduces the capability and technology requirements of the ICT tester to be used and lowers overall capital equipment costs for the production line.

The PT100 has the flexibility to handle future production cycle time reductions or added digital tests (increases in fault coverage) most cost effectively than traditional methods since additional parallel production lines and capital equipment is not needed. The PT100 simply tests and programs more PCBs in parallel with a minimum of additional tester channel cards and fixturing.

CJ Clark is the President and CEO of Intellitech Corporation. He has been the elected chairperson of the IEEE 1149.1 working group and served from 1996 to 2002. Under his direction, the IEEE 1149.1 Standard was re-released with improvements in 2001. CJ is also member of the IEEE 1149.4, IEEE 1532 and P1500 working groups. CJ is co-inventor on one US patent. He has given many papers and presentations at industry conferences and workshops such as the International Test Conference, TECS (Testing Embedded Cores-Based Systems) Workshop, the Board Test Workshop, Ottawa Test Workshop. He is on the VLSI Test Symposium program committee. CJ also serves on the University of New Hampshire College of Engineering and Physical Science (CEPS) Advisory Board. He also serves on the UNH Department of Electrical Engineering Advisory Board.

Mike Ricchetti cis a DFT engineer for ATI Research. He is well known in the Design-for-Test industry for his expertise in DFT methodologies such as core test and BIST. He is a Member of the IEEE and the Computer Society's Test Technology Technical Council (TTTC). Mike has been active as a Working Group member in several IEEE Test Standards, including 1149.1, the 1149.6 Advanced I/O Test Standard and the P1500 Embedded Core Test Standard. He also chairs the TTTC Technical Activities Committee on Silicon Debug and Diagnosis. Mike has over 20 years of experience in Design for Testability and he has authored several papers, and participated in many technical panels, in the area of Design for Test.

References

[1] IEEE Std 1149.1b-1994, “IEEE Standard Test Access Port and Boundary-Scan Architecture”, *Institute of Electrical and Electronic Engineers, Inc*., New York, NY, USA.

[2] Montgomery, Paul, “Non-Volatile Memory Programming on the Agilent 3070”, May 29, 2003. http://we.home.agilent.com/upload/cmc_upload/FlashComp2_052903.pdf

[3] Ricchetti, M. Clark, CJ, Dervisoglu, B., "Method and Apparatus for Providing Optimized Access to Circuits for Debug, Programming, and Test", US Patent 6,594, 802, March 23, 2003. http://www.uspto.gov

[4] Ricchetti, M. Clark, CJ, Dervisoglu, B., "Method and Apparatus for Providing Optimized Access to Circuits for Debug, Programming, and Test", *PCT Patent Application WO0171876*, World Intellectual Property Organization, Geneva, Switzerland, March 23, 2000. http://ep.espacenet.com/

[5] Ricchetti, M. Clark, CJ, "Method and Apparatus for Optimized Parallel Testing and Access of Electronic Circuits", *US Patent Application 2003009715*, US Patent and Trademark Office, Washington, D.C., July 5, 2001.

[6] Clark, CJ, Ricchetti, M., "Method and Apparatus for Optimized Parallel Testing and Access of Electronic Circuits", *PCT Patent Application WO03005050*, World Intellectual Property Organization, Geneva, Switzerland, July 5, 2001.

[7] C.J. Clark, Mike Ricchetti, “Infrastructure IP for Configuration and Test of Boards and Systems”, IEEE Design & Test of Computers, vol. 20, no. 3, May-June 2003, pp. 78-87.

[8] Anonymous, Save Manufacturing Costs Using Intel Flash Memory Enhanced Factory Programming”, Date Unknown, http://www.intel.com/design/flcomp/papers/298344.htm

[9] Anonymous, “Intel Buffered Enhanced Factory Programming Mode improves Programming Performance”, Date Unknown, http://www.intel.com/design/flcomp/papers/BEFP.htm

[10] Paul Montgomery, “Non-Volatile Memory Programming on the Agilent 3070”, May 29th 2003, http://we.home.agilent.com/upload/cmc_upload/FlashComp2_052903.pdf

[11] Anonymous, “Keep PC-board testing from harming low voltage ICs”, Date Unknown, http://www.reed-electronics.com/tmworld/contents/pdf/safetest.pdf

[12] Anonymous, “LightningZ Flash Programming package”, 2001, http://www.teradyne.com/prods/cbt/products/library/z1800s/LightningZ.pdf