In order to meet these objectives, I have championed three new instructions in the IEEE 1149.1 working group, which enable in-situ (in-system) use of silicon instruments. CLAMP_HOLD/CLAMP_RELEASE is a new non-intrusive way of holding the IC pins during operation of silicon instruments. No extra routing around the boundary is required by the designer. This instruction operates on a new test-mode persistence controller so the I/O may remain stable across private and design specific instructions accessing the instruments. The third instruction is IC_RESET which enable on-chip control via JTAG of the reset# or POR# pins. It prevents reset pins from inadvertent toggle via the system during silicon instrument operation. It enables critical system resets between instrument operation without power-down or additional pin access.

There are two more instructions the group has finalized on, INIT_SETUP and INIT_RUN. These address the need for conditioning complex I/Os prior to test modes such as setting voltage levels, differential swing, SERDES protocols and common mode voltages.

The P1149.1-2011 Working Group has defined a re-useable language PDL and BSDL extensions for internal JTAG. You can learn more by taking a look at the presentations I have given at the International Test Conference. I'll update you again in Q2 on the working group progress.


, CEO

Editor's note: CJ was re-elected 1149.1 Chair in a 10-5 vote last December 2010. 1149.1 Elections

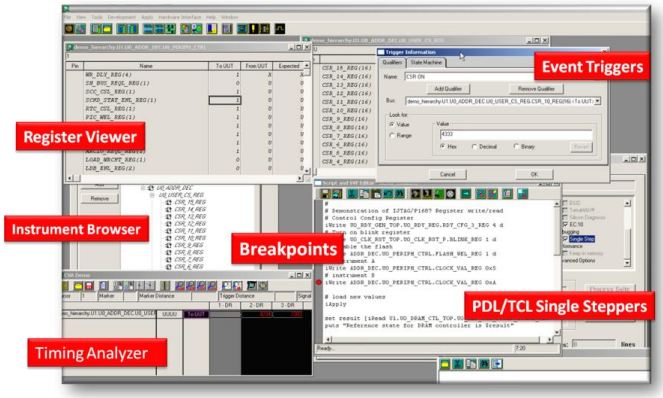
"Using the unique ID in Intellitech ICs for tracking"

By Kareen Lefoley

Each Intellitech device comes with a unique electronic serial number. This serial number can be read from the device via IEEE 1149.1. If the IC package is our 144 BGA or 100 pin TQFP then the serial number is also printed on the package. One advantage of the electronic serial number is that it provides a unique identification of the board or system without a requirement of being physically present to read a bar-code. This enables tracking during certain types of remote/internet based testing. Concurrent testing also can benefit from being able to skip the bar-code scanning step.

Each device also contains read only information on the customer ID, ordering ID (the entity which placed the order), unique 128 bit number, and secure hash. Using one Intellitech IC on your PCB can prevent cloning of your product. You can learn more and retrieve serial number histories at Electronic Silicon ID.

NEBULA – Surpasses 200 free downloads!



This quarter, NEBULA reached over 200 free users. If you haven't downloaded the free NEBULA software for P1149.1-2011 and P1687, now is the time. After five hundred downloads it will no longer be free. You can use NEBULA to write instrument PDL/Tcl and validate against simulation models in VCS. When you have real silicon, you can execute your PDL/Tcl using a low cost Xilinx USB pod.

What do you get with NEBULA?

- BSDL compiler/database creator
- P1149.1-2011 BSDL extensions
- Hierarchical internal register viewer
- Pin/Register spreadsheet views
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- SVF Application (program FPGAs/CPLDs)
- Tcl/PDL scripting language