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IEEE 1149.1™-2013 DESIGNED TO SLASH ELECTRONICS INDUSTRY COSTS BY ALLOWING TEST RE-USE THROUGHOUT INTEGRATED CIRCUIT LIFECYCLE

Newly revised IEEE 1149.1 'JTAG' standard intended to enable transfer of critical domain expertise from intellectual property (IP) providers to downstream customers

PISCATAWAY, N.J., USA, 17 June 2013 – IEEE, the world's largest professional organization advancing technology for humanity, today announced IEEE 1149.1™-2013 "Standard for Test Access Port and Boundary-Scan Architecture." IEEE 1149.1-2013—commonly known in the industry as "JTAG," for "Joint Test Action Group"—is intended to dramatically lower electronics industry costs by enabling test re-use across all phases of the integrated circuit (IC) lifecycle via vendor-independent, hierarchical test languages.

The revision of IEEE 1149.1, the first for the standard since 2001, allows critical domain expertise for intellectual property (IP)—how to configure a serializer/deserializer (SERDES) for loopback testing, for example—to be transferred in a computer-readable format from the IP designer to IC designers and, in turn, to designers of printed circuit boards (PCBs) and to test engineers, gradually magnifying industry cost savings along the supply chain. The cost savings for the electronics industry that IEEE 1149.1-2013 is intended to unlock are estimated to be in the billions of dollars.

IEEE 1149.1-2013 specifies a new hierarchical Procedural Definition Language (PDL)—a standard test language based on Tcl, and hierarchical extensions to the original Boundary Scan Description Language (BSDL) to describe on-chip IP test data registers. Eight new optional IC instructions provide a foundation for configuring I/Os for board test, mitigating false failures when re-testing the IC at the board level and correlating the results back to wafer level test through an Electronic Chip ID.

"IEEE 1149.1-2013 is poised to have a major impact on how business is done across the electronics industry—from IP providers to silicon vendors to system integrators—as it is designed to eliminate inefficient engineering," said C.J. Clark, chair of the IEEE 1149.1 working

group and chief executive officer of Intellitech. “The IP provider can document the IP test interface and how to operate the IP in an English-like language—just once, for all ICs. Software tools then re-target this documentation at the IC and board level for tests. In revising IEEE 1149.1, the working group focused on two things: lowering industry costs through the new PDL language and enabling test re-use over the lifecycle of an integrated circuit. Now, for the first time in our industry, a standard overcomes the 'Tower of Babel' language differences and enables on-chip tests to be re-used and correlated across IC, board and field automatic test equipment (ATE). It's easy to see how the cost savings propagate across vendors and buyers in the IC supply chain.”

IEEE 1149.1-2013 provides critical synergy with two other important industry standards. IEEE 1149.1-2013 supports segmented on-chip test data registers that cross power domains specified by IEEE 1801™-2013 “Standard for Design and Verification of Low Power Integrated Circuits”. IEEE 1149.1-2013 enables descriptions and operation of IP accessible via IEEE 1500™-2005 “Standard Testability Method for Embedded Core-based Integrated Circuits” structures; IEEE 1500 is frequently used for production IC testing. IEEE 1149.1-2013 domain segmentation adds new capability to the IEEE 1500 Wrapper Serial Ports.

“The new features of IEEE 1149.1-2013 address the many challenges in describing and managing chips with complex programmable I/Os or chips with multiple power domains. Private instructions and test data registers can be documented and tool support for them can be automated,” said Carol Pyron, vice chair of the IEEE 1149.1 working group and senior member of technical staff with Freescale Semiconductor.

Clark added: “For more than 23 years, IEEE 1149.1 compliance has been an important requirement for buyers of application-specific IC (ASICs) and system-on-chip (SoCs). IEEE 1149.1-2013 extends this for buyers of IP. All customers can be assured of ease of use and re-use of tests.”

A large cross section of representatives from IP providers, silicon providers, original equipment manufacturers (OEMs) and test providers participated in the IEEE 1149.1-2013 revision project.

IEEE 1149.1-2013 is available for purchase at the IEEE Standards Store.

For more information about IEEE 1149.1, please visit http://standards.ieee.org/findstds/standard/1149.1-2013.html.

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