

**Developing for 1149.1-2013
with Intellitech
NEBULA Software**



How does NEBULA for 1149.1-2013 help?

- **Control and Configure SERDES I/O**
 - **Set I/O differential swings for IC ATE test**
 - **Program I/O XCVERs for board interconnect test**
 - **Disable AC Coupling**
- **Characterize early system FR4/PCB designs**
 - **Execute at-speed ecosystem tests on PCBs**
 - **Run DDR interconnect test**
 - **Execute SERDES at-speed interconnect**
- **Perform lab/benchttop IC characterization**
 - **Run on-chip BIST tests**
 - **Measure on-chip droop voltage (inject droop)**
 - **Enable/Disable power domains**
 - **Check interconnect across TSVs**

NEBULA for 1149.1-2013 Development

The screenshot displays the NEBULA development environment with several tool windows open:

- Register Viewer:** A table showing register information with columns for Pin, Name, To UUT, From UUT, and Expected. The table lists registers such as WR_DLY_REG(4), SH_BUS_REQ_REG(1), SCC_CSL_REG(1), SCND_STAT_ENL_REG(1), RTC_CSL_REG(1), PTC_WEL_REG(1), PTC_CSL_REG(1), LOAD_WRCNT_REG(1), and LDB_ENL_REG(2).
- Instrument Browser:** A tree view showing the hierarchy of UUT components, including U0_ADDR_DEC, U0_USER_CS_REG, and various CSR registers (CSR_6_REG to CSR_15_REG).
- Trigger Information:** A dialog box for configuring event triggers. It shows a Name of "CSR ON" and a Bus of "demo_hierarchy.U1.U0_ADDR_DEC.U0_USER_CS_REG.CSR_10_REG[16] <To UUT>". The "Look for" section is set to "Value" with a value of "4333" and radio buttons for "Hex", "Decimal", and "Binary".
- Script and SVF Editor:** A text editor window containing a script for demonstrating IOTAG/P1687 register write/read operations. The script includes comments and commands like `iWrite U0_RDY_GEN_TOP.U0_RDY_REG.RDY_CFG_3_REG 4 d` and `iWrite ADDR_DEC.U0_PERIPH_CTRL.CLOCK_VAL_REG 0xA`.
- Timing Analyzer:** A window showing a signal trace for "demo_hierarchy.U1.U0_ADDR_DEC.U0_USER_CS_REG". It includes columns for Marker, Marker Distance, Trigger Distance, and Signal, with a signal value of 4234 and 7363.

Register Viewer

Event Triggers

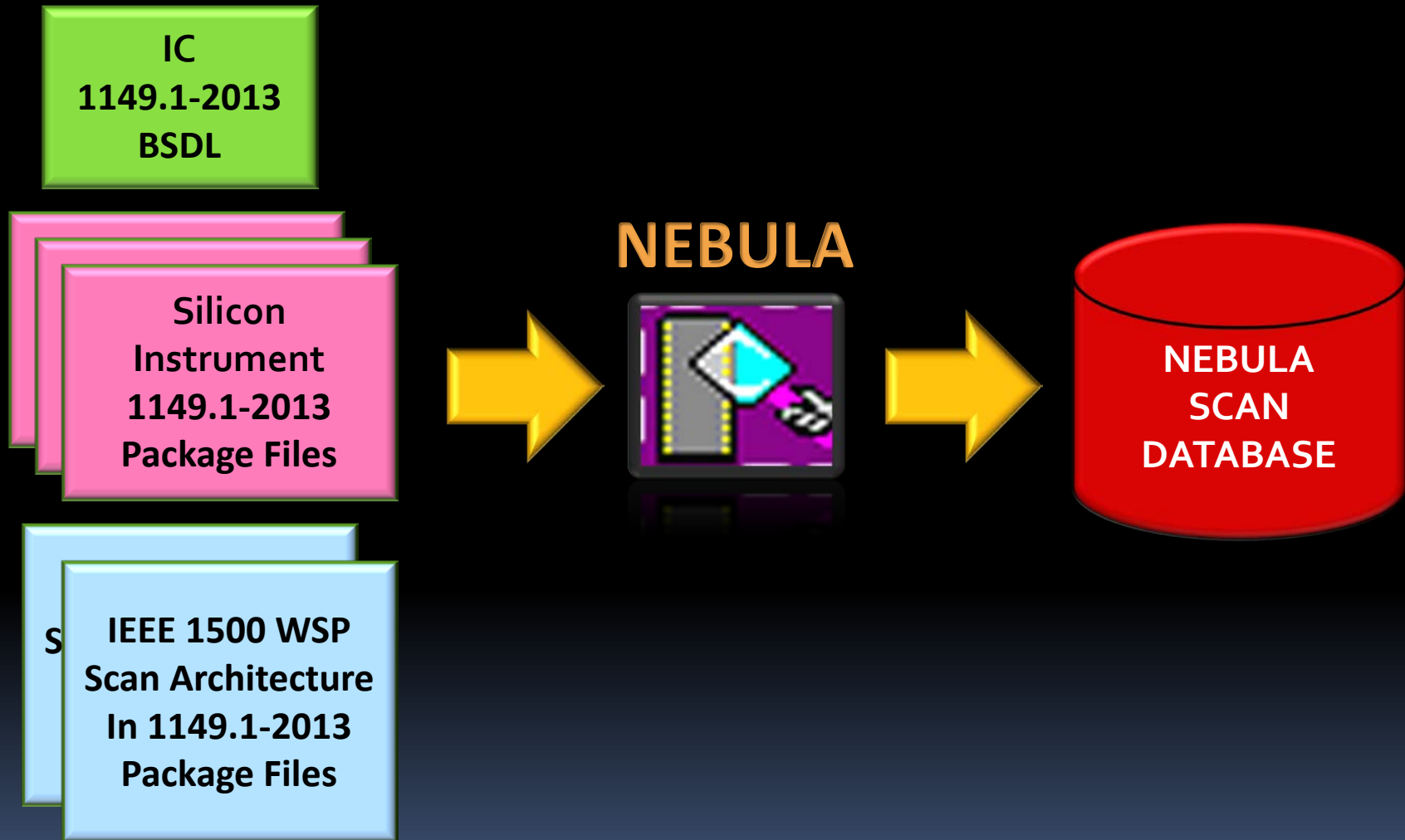
Instrument Browser

Breakpoints

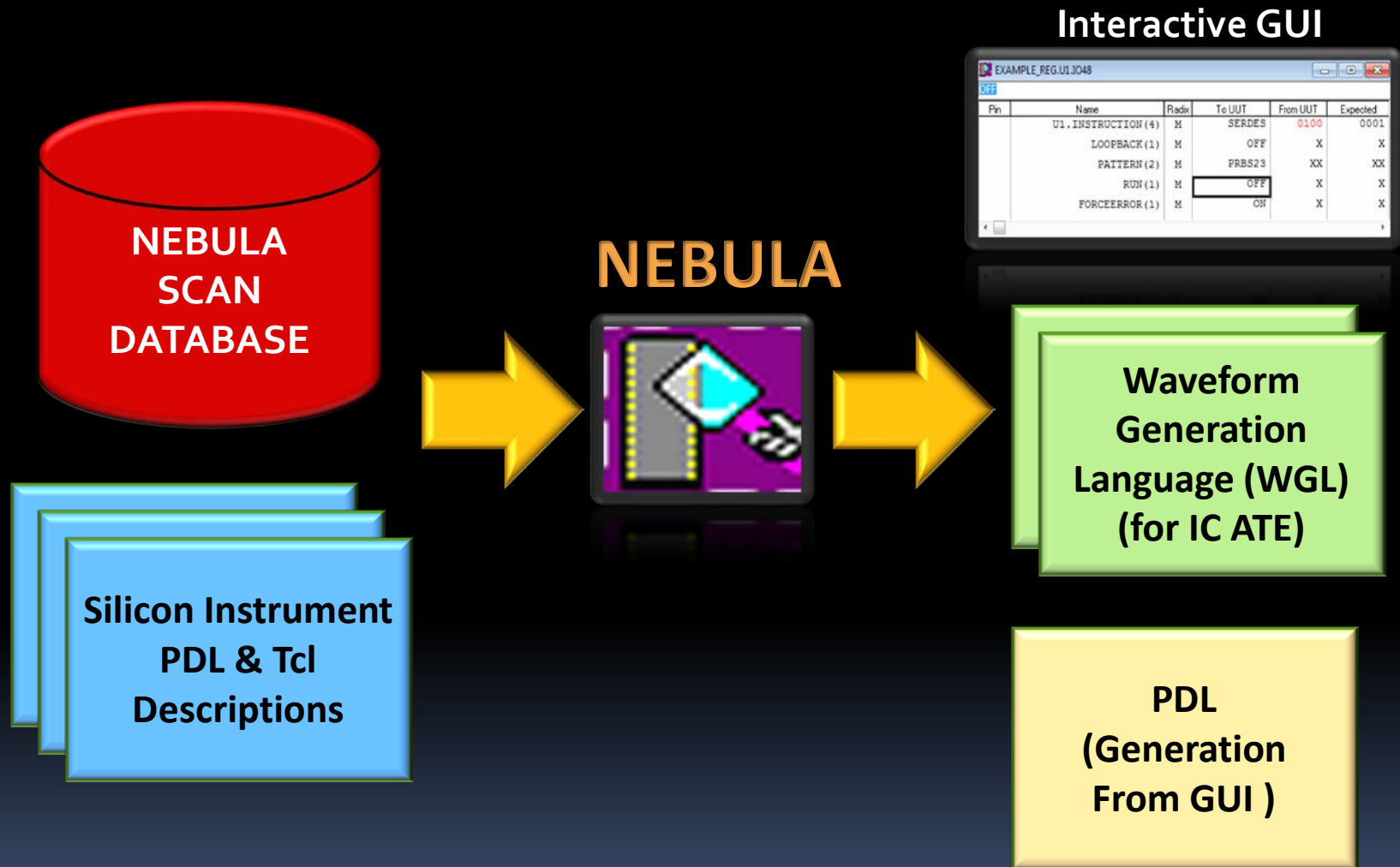
PDL/TCL Single Steppers

Timing Analyzer

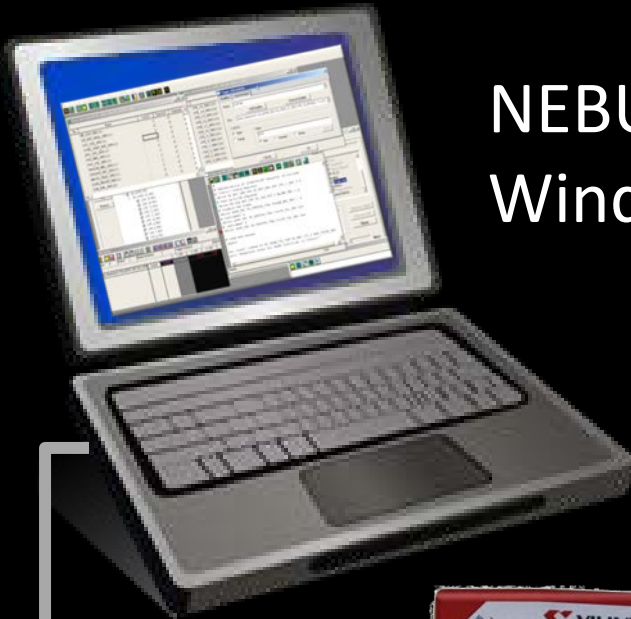
NEBULA Software Flow



1149.1 PDL and Tcl operate on Scan Database



Typical Lab Setup

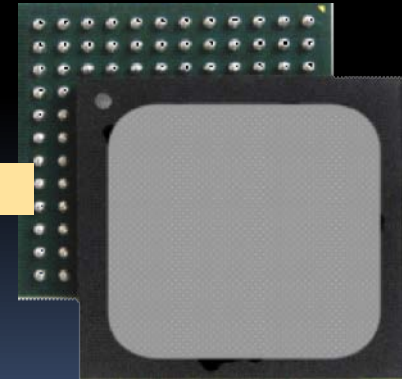


NEBULA running on
Windows7 Laptop

SoC or FPGA

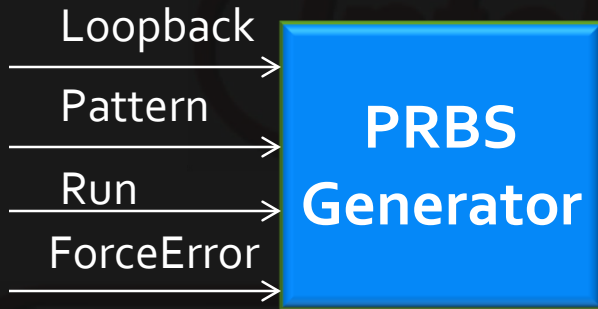


JTAG cable



FPGA USB
JTAG Controller

NEBULA reads 1149.1-2013 attributes



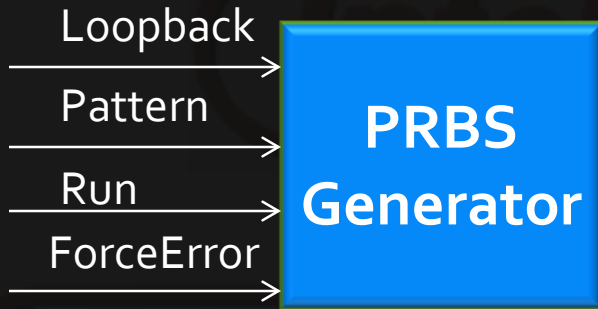
- Describe Interface to IP w/o TAP
- Description is "packaged" in compliant IEEE 1149.1-2013 package file
- Describe just interface + mnemonics
- Machine readable

```
Attribute REGISTER_MNEMONICS of SERPRBS : package is
"OnGroup      (ON (1), OFF (0)), " &
"PatGroup     ( PRBS31(1), PRBS23 (2), PRBS7(3) );"
```

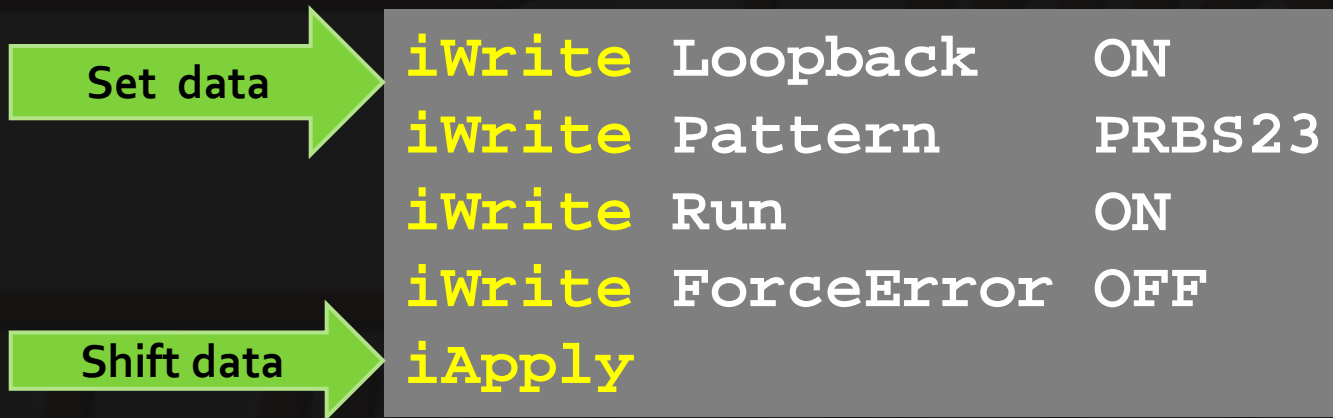
```
Attribute REGISTER_FIELDS of SERPRBS : package is
```

```
"PRBS [5] ( "&
"(Loopback   [1] IS (4) DEFAULT(OnGroup(ON))), " &
"(Pattern    [2] IS (3,2)  DEFAULT(PatGroup(PRBS7)) ), " &
"(Run        [1] IS (1)    SAFE(OnGroup(OFF)) ), " &
"(ForceError [1] IS (0)) DEFAULT(OnGroup(OFF));"
```

NEBULA reads PDL/Tcl control sequences



Procedural Description Language
- new vectorless re-targetable
language for describing IP operation

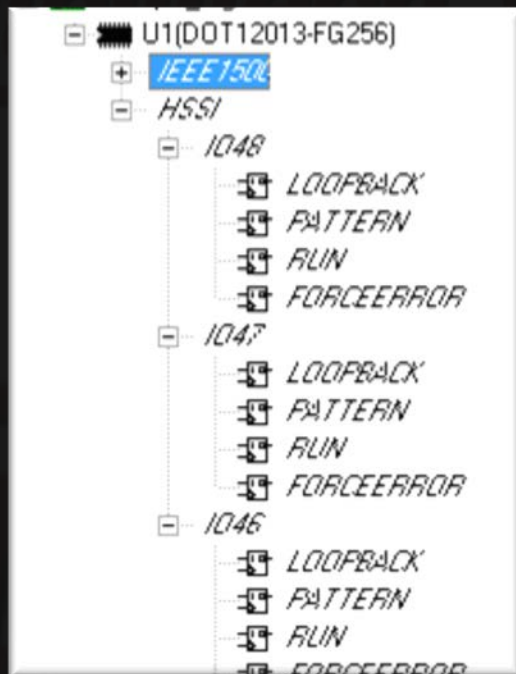
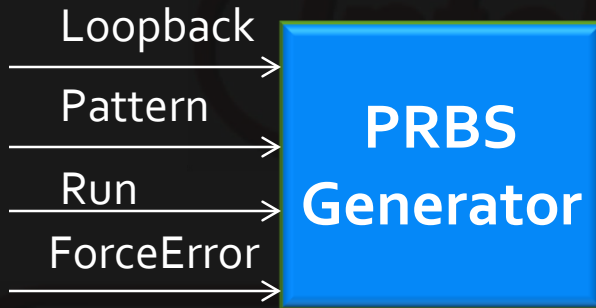


Format: **<iWrite >** <Register> <value or mnemonic>

NEBULA software reads IP package files

Creates hierarchy from IP to IC level TAP

Interactive display



A screenshot of a configuration window titled "EXAMPLE_REG.U1.IO48". The window shows a table of configurations for a specific pin. The "To UUT" column has a dropdown menu set to "OFF". A mouse cursor is pointing at the "OFF" option.

Pin	Name	Radix	To UUT	From UUT	Expected
	U1 . INSTRUCTION (4)	M	SERDES	0100	0001
	LOOPBACK (1)	M	OFF	X	X
	PATTERN (2)	M	PRBS23	XX	XX
	RUN (1)	M	OFF	X	X
	FORCEERROR (1)	M	ON	X	X

Example Silicon Instrument GUIs in NEBULA

s3an_demo.U2.DAC1 :: LTC2624

LTC2624 4-Channel 12-bit Digital-to-Analog Converter

Channel	Vref	VrefLo	Vout
Ch A	3.30	0.00	2.50
Ch B	3.30		1.20
Ch C	3.30		3.30
Ch D	3.30		1.80

s3an_demo.U2.ADC1 :: LTC1407-1

LTC1407-1 2-Channel 12-Bit Analog-to-Digital Converter

Channel	Vref	Voltage
Ch 0	1.65	0.75 V
Ch 1	1.65	2.90 V

Read ADC

s3an_demo.U2.AMP1 :: LTC6912-1

LTC6912-1 2-Channel Programmable Gain Amplifier

Gain	Ch A	Ch B	Verify Data	
ZERO	ZERO	ZERO	X_2	X_5
X_1	X_1	X_1		
X_2	X_2	X_2		
X_5	X_5	X_5		
X_10	X_10	X_10		

Update