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PRESS RELEASE

New IEEE 1149.1-2012 JTAG standard, supporting re-usable IC test structures passes ballot

Anaheim, CA - ITC - International Test Conference - November 7, 2012 —Intellitech Corporation announced today that the proposed IEEE 1149.1-2012 JTAG standard has reached consensus with an eighty-five percent approval in a recent IEEE ballot. The standard incorporates industry best practices for enabling IC test re-use from silicon to systems. Structural and procedural description languages have been standardized to support re-use of on-chip infrastructure IP blocks such as MemoryBIST, IOBIST, Logic BIST, SERDES PRBS, droop injectors, temperature and voltage monitors. The hierarchical description extensions to 1149.1 BSDL allow self-contained infrastructure IP descriptions which can then be instantiated at higher levels. A hierarchical documentation language PDL, Procedural Definition Language based on the open source Tcl allows the IP vendor to describe the necessary steps to configure the IP via JTAG, initiate tests and retrieve the results. The standard describes eight foundational instructions which provide support for programming I/O, tracking die through a unique ID, and executing on-chip tests in-situ without the integrity of the tests being impacted by the IC ecosystem. The standard reaches a critical balance for the system integrator, the IC purchaser and the IC vendor. There are rules and documentation requirements which protect the system integrator and rules which protect the IC vendor from false indictments of the IC in the field.

IEEE 1149.1-2012 now describe IEEE 1500 Wrapper Serial Port architectures and provides 1149.1 TAP access to those IEEE 1500 serial ports. A new synergy exists between the standards

where 1149.1-2012 domain control enables the fixed IEEE 1500 bus to be segmented through power domains or stacked die. The capability enables IEEE 1149.1-2012 as "3D-SIC ready"; a stack using 1149.1 and 1500 can be described with a single BSDL and a package file for each 1500 wrapped die. Since major EDA companies support IC test through IEEE 1500, incremental changes can be made to EDA tools to take advantage of the new on-chip structures and higher level of abstraction provided by 1149.1 BSDL and PDL. These languages would not replace but complement IEEE 1450.6 CTL.

"I am very pleased with the work the Working Group has accomplished. There were a number of critical decisions the working group made that resulted in a robust standard that will drastically reduce test related engineering while enhancing IC and system test capabilities," said CJ Clark, Intellitech CEO and chair of IEEE 1149.1. "Our ballot group consisted of a large cross section of the industry. Ballot members with affiliations from Alcatel-Lucent, AMD, ARM, Cadence, Cisco, Freescale, Intel, Intellitech, NXP, ST Microelectronics, Synopsys, Texas Instruments and Teradyne all voted with approval," he continued.

"Intellitech has been a pioneer in the use of 1149.1 with silicon instruments, laying the fundamental groundwork of re-usable register definitions, mnemonics and use of Tcl for procedures in the late 1990s back when many were focused on the boundary-scan half of the 1149.1 standard. Naturally, we continue to maintain our leadership position with NEBULA and Eclipse tools which support the new capabilities of the standard. At the same time we will be helping rapidly grow the use of 1149.1-2012 through a free BSDL compiler compliant with the new standard at http://www.intellitech.com/BSDL and the freely available NEBULA product for accessing internal JTAG using 1149.1-2012 available at http://www.intellitech.com/ijtag," Clark concluded.

Additional information can be found at the IEEE website http://grouper.ieee.org/groups/1149/1/

About Intellitech

http://www.intellitech.com/company/about.asp

Definitions

BSDL - Boundary Scan Description Language. A formal description language for scan registers that is part of IEEE 1149.1 since 1994

BIST - Built In Self-Test. Logic design to perform a test and return a result with minimal stimuli from outside the IC.

CTL - Core Test Language

ECID - Electronic Chip Identification

IEEE - Institute of Electrical and Electronic Engineers

IEEE 1500 - Standard for Embedded Core Test

Infrastructure IP - On-chip IP which are Design-for-Yield and Design-for-Test structures used for enhancing yield, enhancing IC test or performing external IC ecosystem test at the system level.

TAP - Test Access Port. The dedicated serial port on all IEEE 1149.1 compliant pins which gives access to all scan based structures.

Tcl - Tool Command Language

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