P1149.10 High Speed JTAG -debug using a fire hose rather than a straw

CJ Clark, Intellitech CEO

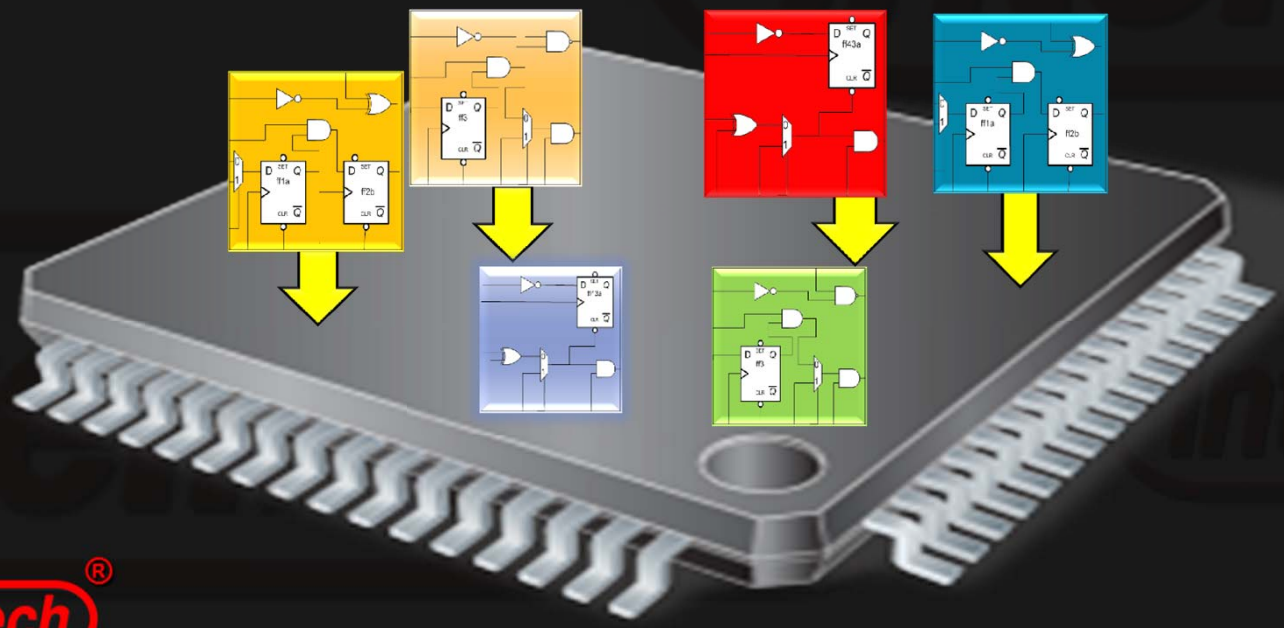
Chair, P1149.10
Past Chair, IEEE 1149.1-2013

- Some basics
  - using 1149.1-2013
- What's coming
  - P1149.10 High Speed JTAG

IEEE 1149.1-2013 Executive Summary

- Standardizes a plug-n-play test interface for Silicon Instruments

- PVT monitors
- On-chip Logic Analyzer
- On-chip transactors
- "JTAG2Bus" masters
- Scan-dump triggers
- Memory BISR
- SerDes BIST
- Hardware assertion checkers
- Instruction Footprint recorders
- Clock Step/Pause



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WORM - Write Once Read Many

Through the standard hierarchical English-like languages of 1149.1-2013, IP designers can transfer critical expertise to IC designers and others

One 1149.1-2013 compliant SII gets leveraged across hundreds of engineers
One 1149.1-2013 compliant IC may have hundreds or thousands of IP

SII Designer | IC Designers | OSAT Engineers | PCB Designers | Test Engineers

SII Domain Expertise

Closest to source → Furthest

Total Industry Cost Savings $

OSAT = Out Sourced Assembly & Test

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1149.1-2013 Solution: Standardize SII documentation

AXI4 Master example "SI package"

```
attribute REGISTER_MNEMONICS of AXI4 : package is
 "Mode (Fixed      (0B00) <Checkerboard>, "&
 "      Incr       (0B01) <GALPAT >, " &
 "      Wrap       (0B10) < March Algorithm >, "&
 "      Reserved   (0B11) < Moving Invert >), "&
 "Run  (Start     (1),   " &
 "       Loop      (2), " &
 "      Stop      (3) ), " &
 "Type  (Write       (0),   " &
 "        Read       (1); "

attribute REGISTER_FIELDS of AXI4 : package is
"TDRSEG [36]( "&
 "( Type[2] IS (36) DEFAULT(Type (Write)) NOUPD ),"&
 "( Mode[2] IS (35 DOWNTO 33) DEFAULT(Mode (Fixed)) NOUPD ),"&
 "( Run[2]   IS (33 DOWNTO 32) DEFAULT(Run  (Stop )) ), "&
 "( Data[32] IS (31 DOWNTO 0) ) )";
```

AXI4 Master

TDR Segment

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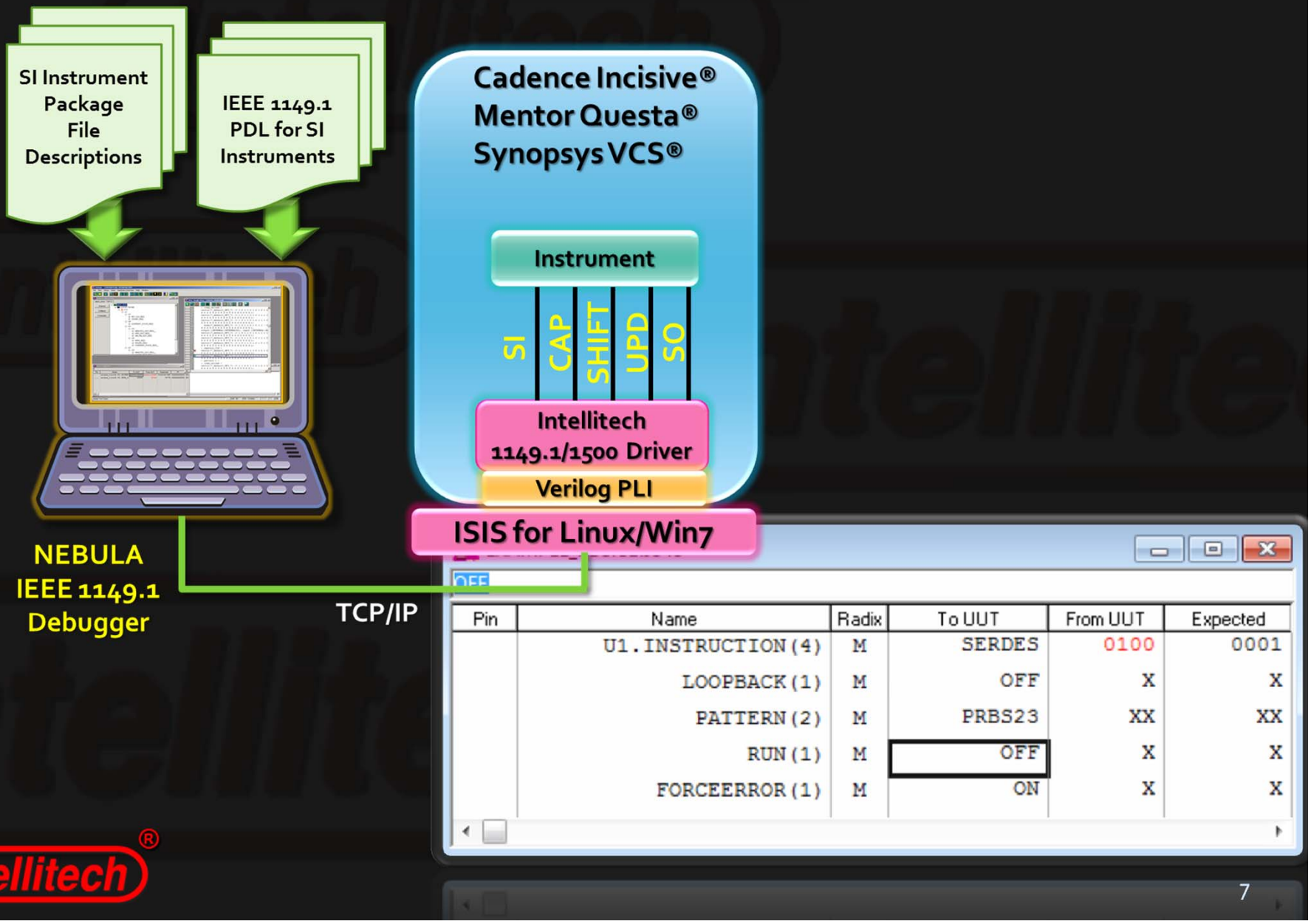
1149.1-2013 Solution: Standardize IP documentation

PDL Description of how to operate AXI4 Master

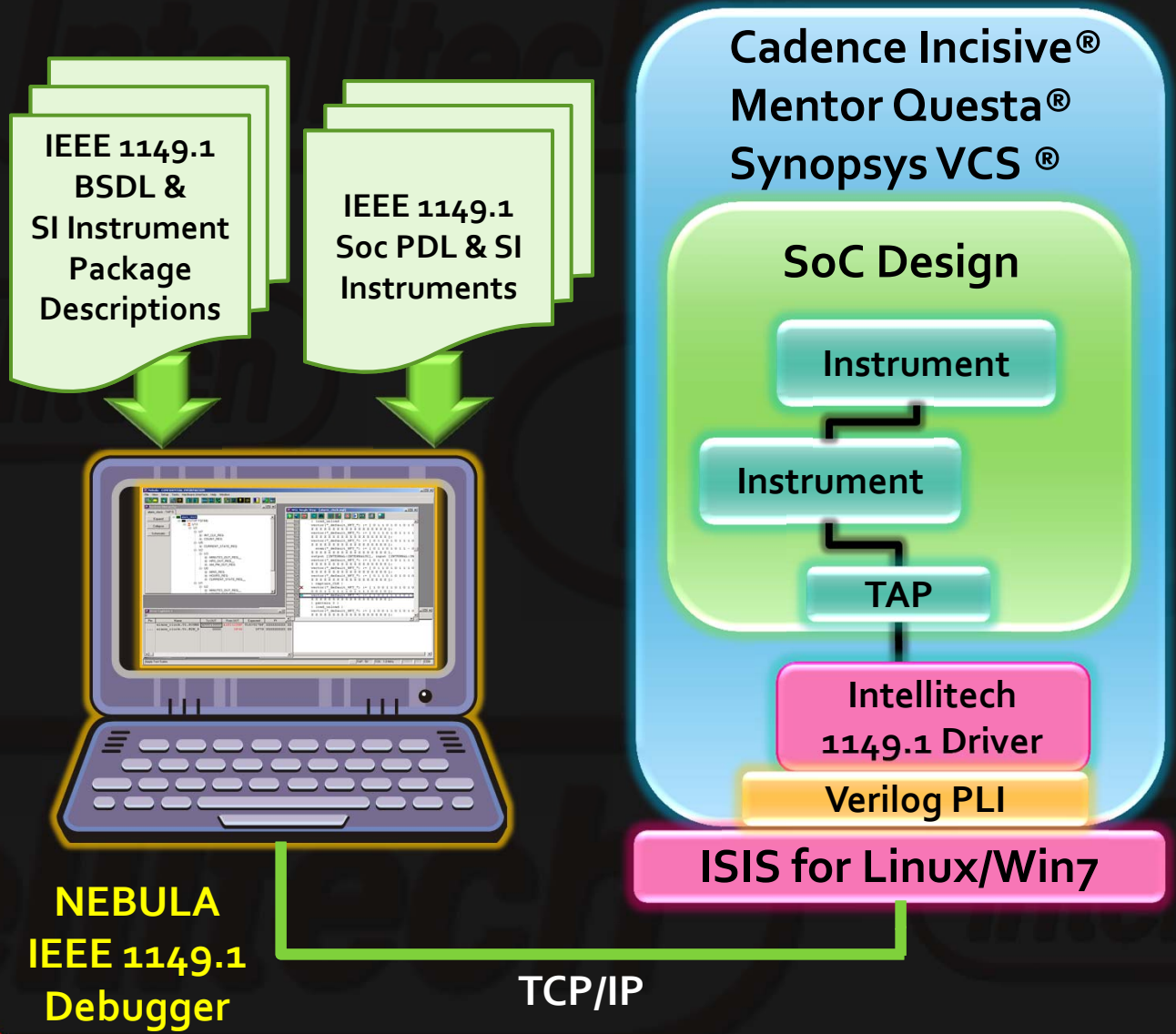
```
# AXI4.pdl
iPDLLevel 0 -version STD_1149_1_2013
iProcGroup AXI4
iProc Run_AXI4 -export {addr data type}

   iWrite data $data
   iWrite type  $type
   iWrite mode  Fixed
   iWrite addr  $addr
   iApply
   iRunLoop 10000 -sck $clk
}
```

Validate SII Package & PDL stand-alone



Validate at top level with all SI instruments

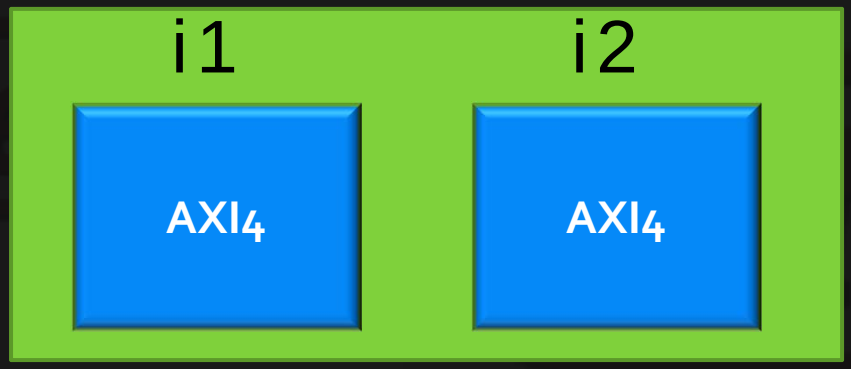


Tools re-target register access for the user

Package AXI4

```
iWrite Data 0x11_22_33_44_55_66_77_88
```

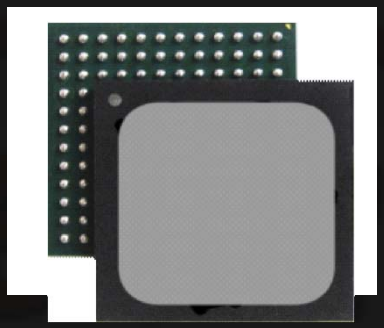
BOTH



Package AXI4
Package BOTH

Tool converts to:

```
iWrite BOTH.i1.Data $data
```



Package AXI4
Package BOTH
IC BSDL

Tool converts to:

```
iWrite U1.BOTH.i1.Data $data
```

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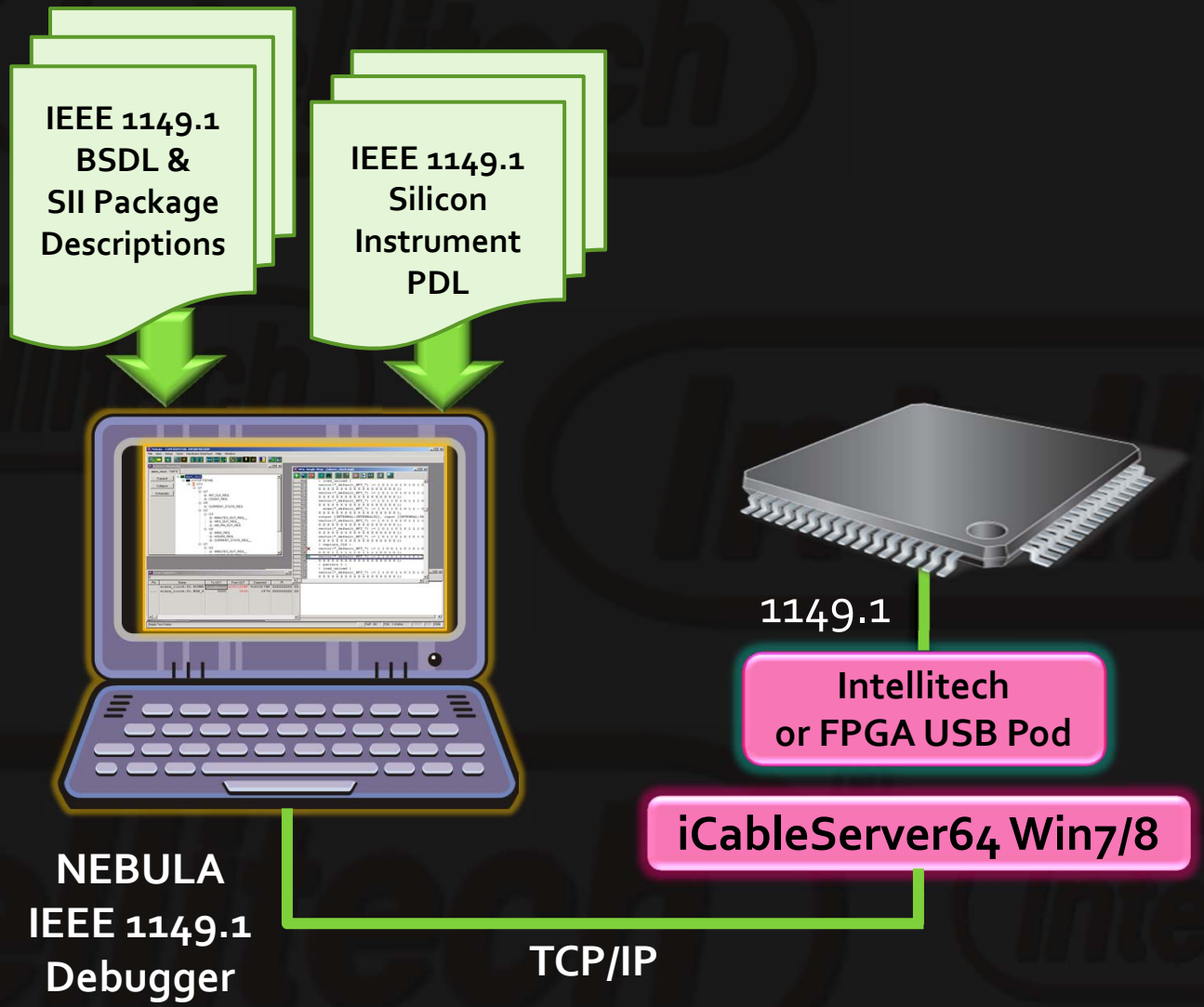
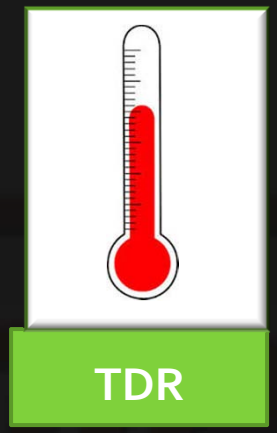
Re-use all with first Silicon



Analog Instrument s via IEEE 1149.1-2013 PDL

- Silicon Instrument doesn't necessarily have an 'expected' value
- Customer wants pre-engineered solution
  - Instrument and software 'plug n play' via TAP *including translation to human Understandable value* (not 1's and os)
  - Customer needs TAP based CPU emulation AND access to silicon instruments
- IP provider desires to develop pre-engineered solution
  - Need robust language (math operations, logical operations, etc) needed to make sense of data scanned out

Temp Monitor



$$Voltage = 10 \times \frac{\kappa T}{q} \times \ln(10)$$

In IEEE 1149.1-2013 PDL:

```
iProc read {} {
iGet registerValue
set temp =  ([$registerValue x 503.975]  / 4096) - 273.15
Return $temp
}
```

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P1149.10 High Speed JTAG

Objectives:

Re-use PDL

Re-use SII package structual info

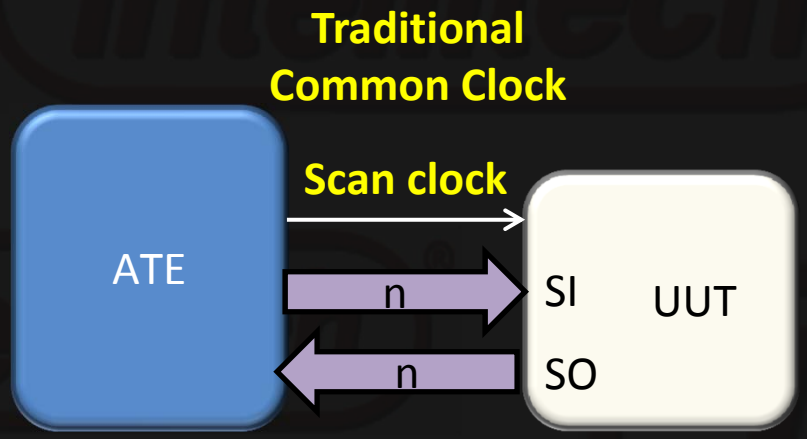
In-situ SoC test/debug

Reduce power

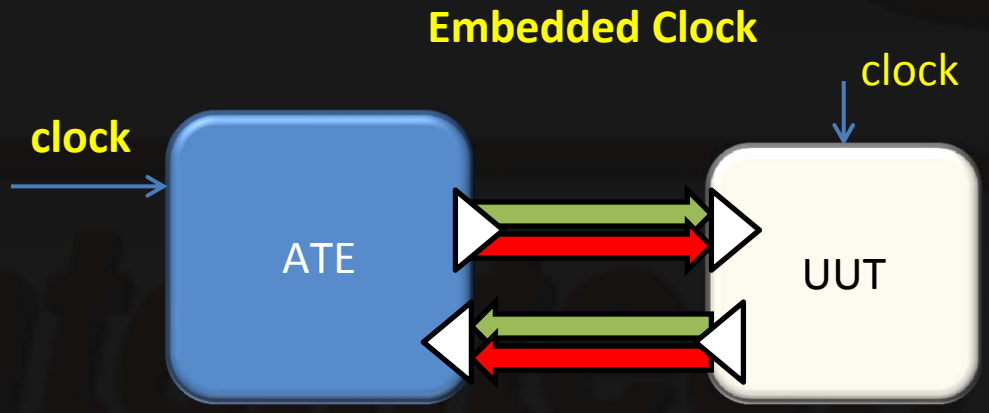
Reduce test times

Reduce touch-downs with Virtual Scan-Channels

P1149.10 motivations:
Traditional Common Clock reaching a ceiling?



- N scan channels
  N is pin limited
- 2*N touch downs
- SCLK > 100Mhz
- Skew challenges
- Tester resource
- Compression
  Silicon debug complexity



- M scan channels
  M >> N
  Slow clock/Low power
- 5+4 Touch downs
- Scales with new PHY
- Reduce compression needs
- Bond multiple channels

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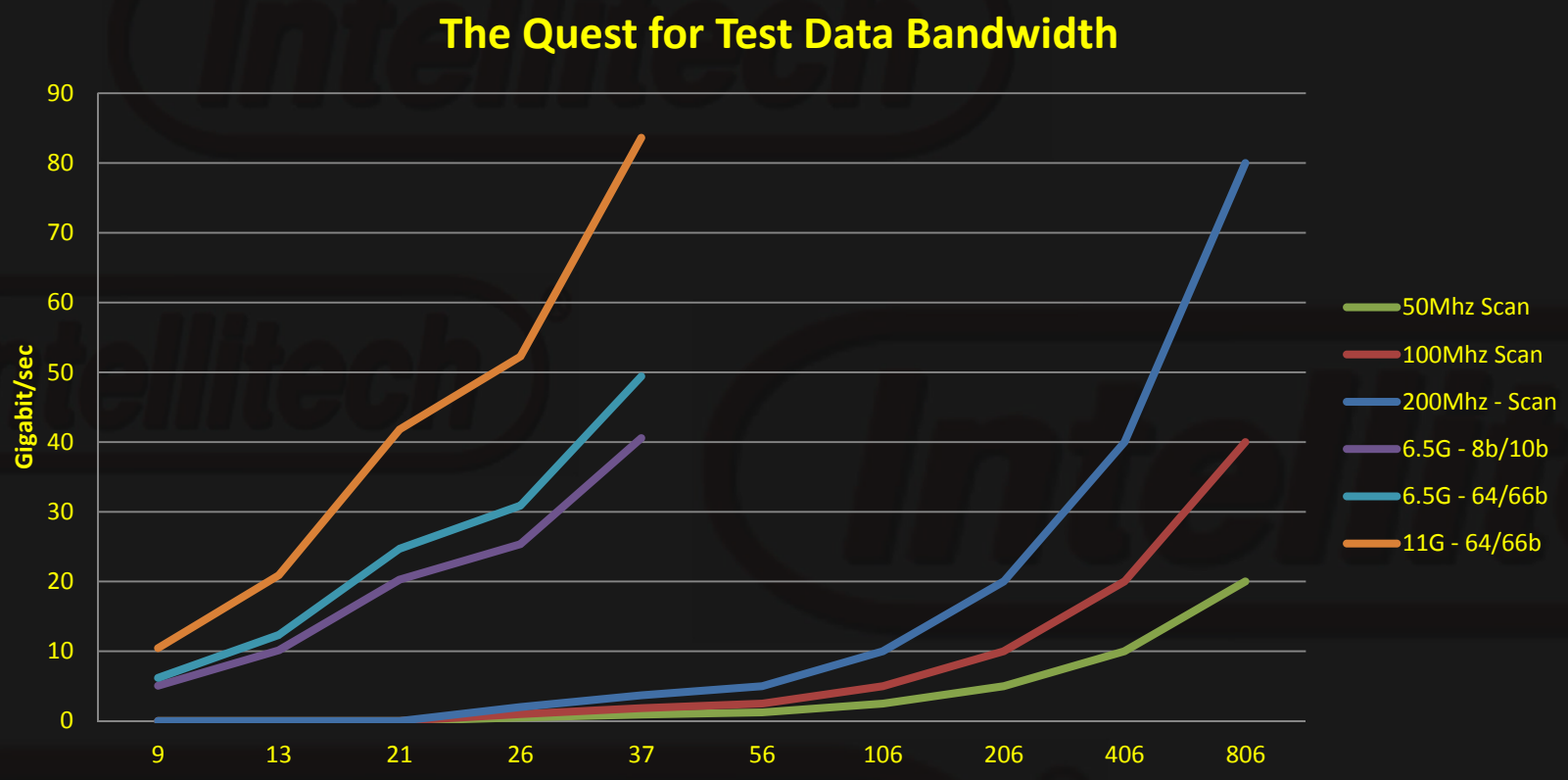
Common Clock = 80G/sec = 400 chains, 806 pins and 200Mhz operation
Embedded Clock SERDES = 80G/sec = User Defined chains, 37 pins and user defined Mhz



SI/SO+TAP+CLK		9	13	21	20	37	50	100	200	400	800
Chains		X	X	X	10	X	25	50	100	200	400
Tester Chan		9	13	21	26	37	56	106	206	406	806

SERDES = 4 pins + 4 pin TAP + clock. Channel bonding is used to have 2,4 and 8 Serdes lanes.
5 SERDES lanes just included for comparison purposes.
Bandwidth adjusted for encoding bit loss and 2% overhead of packet

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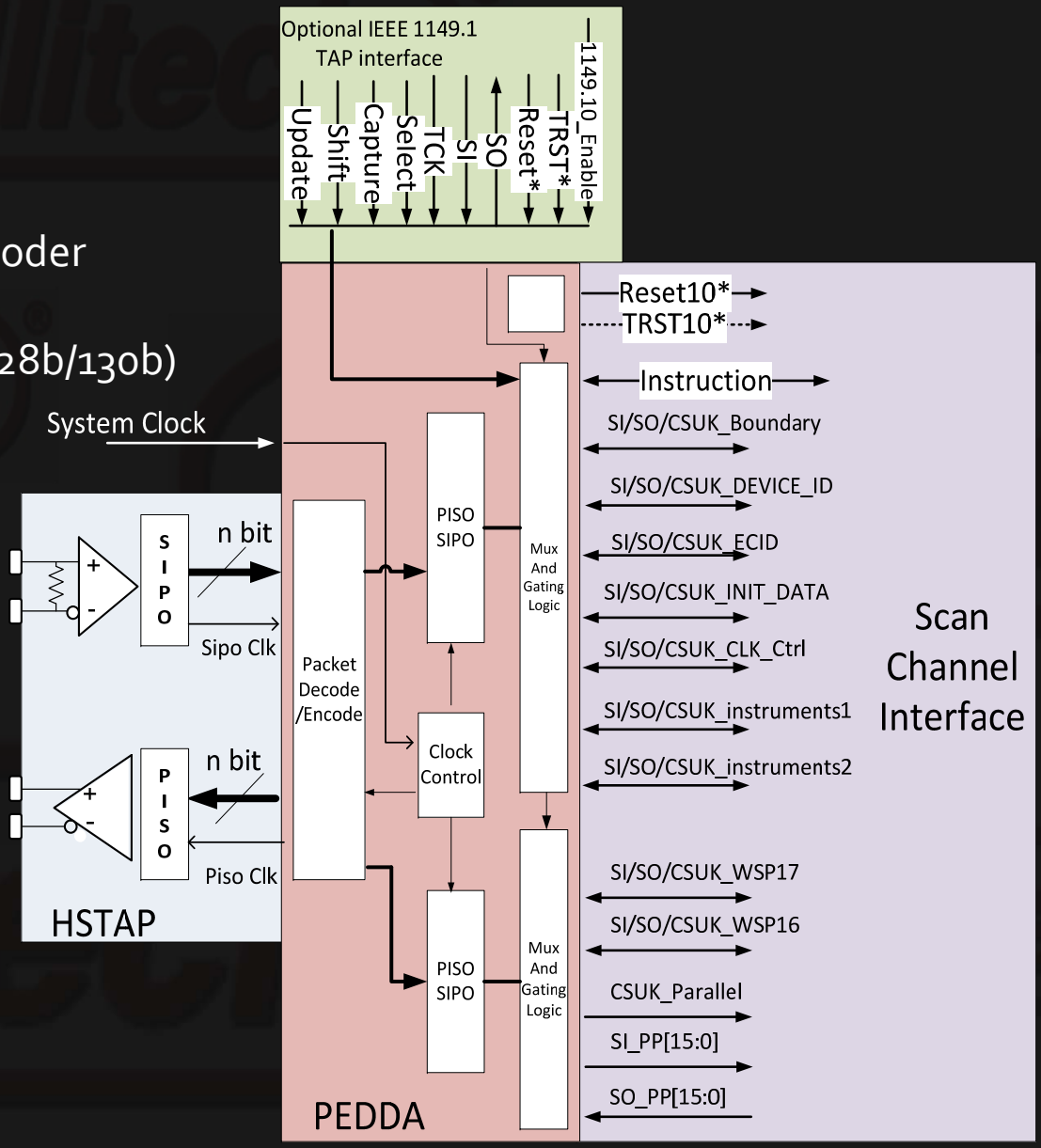
P1149.10 example diagram

HSTAP - High Speed TAP
PEDDA - Packet Encoder/Decoder

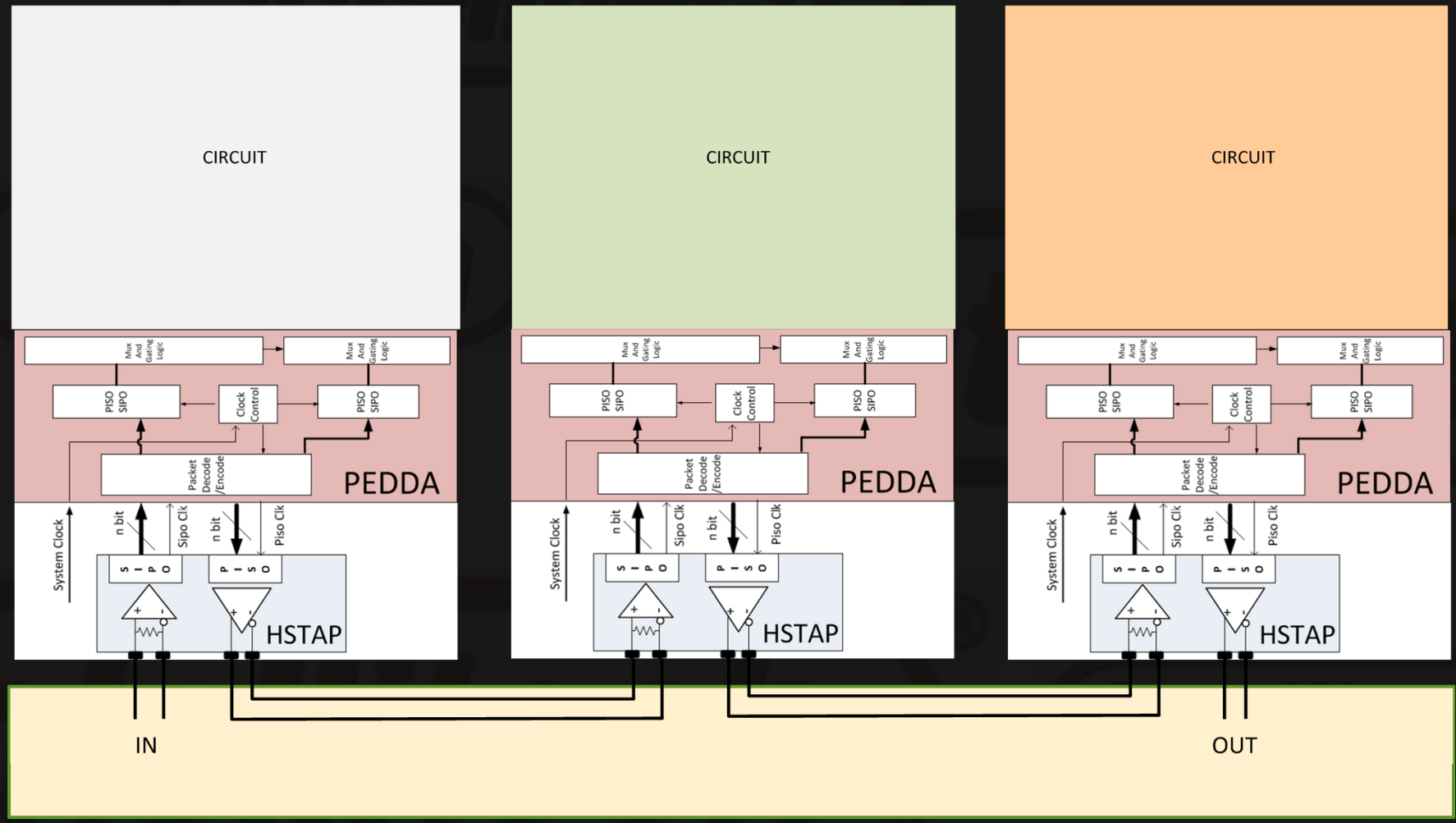
Encoding (8b/10b, 64b/66b, 128b/130b)

Scan-chains
For Test
For Silicon Debug

Share Mission SERDES
Optionally use TAP to
configure/enable SERDES



Daisy Chain HSTAPS/PEDDA
- connect within die or connect die



What about Nexus 5001? That uses SERDES too
- Very Application specific/CPU specific

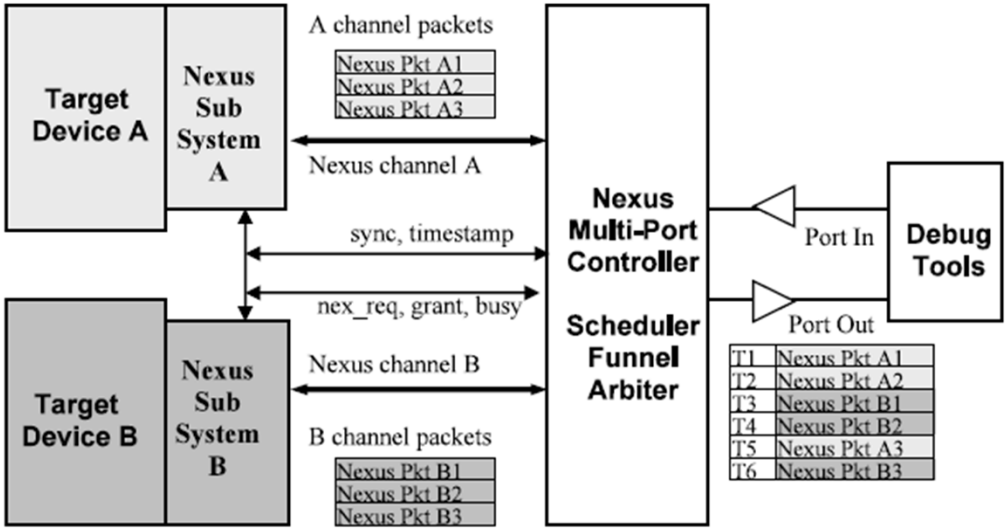


Figure 1: Integrated Nexus 5001 Subsystems with Interwoven Packets

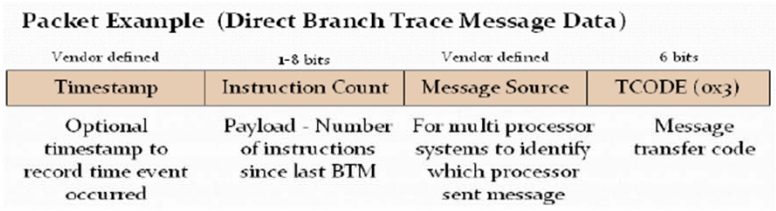


Figure 2: An exemplary Nexus 5001 Packet

Packets:
CPU debug focused
Single IC (no chaining)
No application of test data
No PDL re-use
No SPI / alternate serial

Neil Stollon, HDL Dynamics 2012 Nexus forum

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Packet Commands

CONFIG- Enable uninitialized P1149.10 interface to be enumerated to 'n'

TARGET <n> - specify where packets go

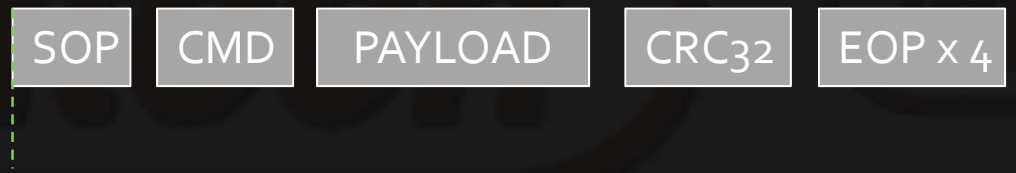
RESET - Assert reset* or TRST* (internally different signals)

RAW - Enable Interface in a RAW data mode (suitable for BER testing)
Data is not processed by packet processor subsequently and all RX data is sent to TX

SCAN - Interleaved IR/DR Scan Packet

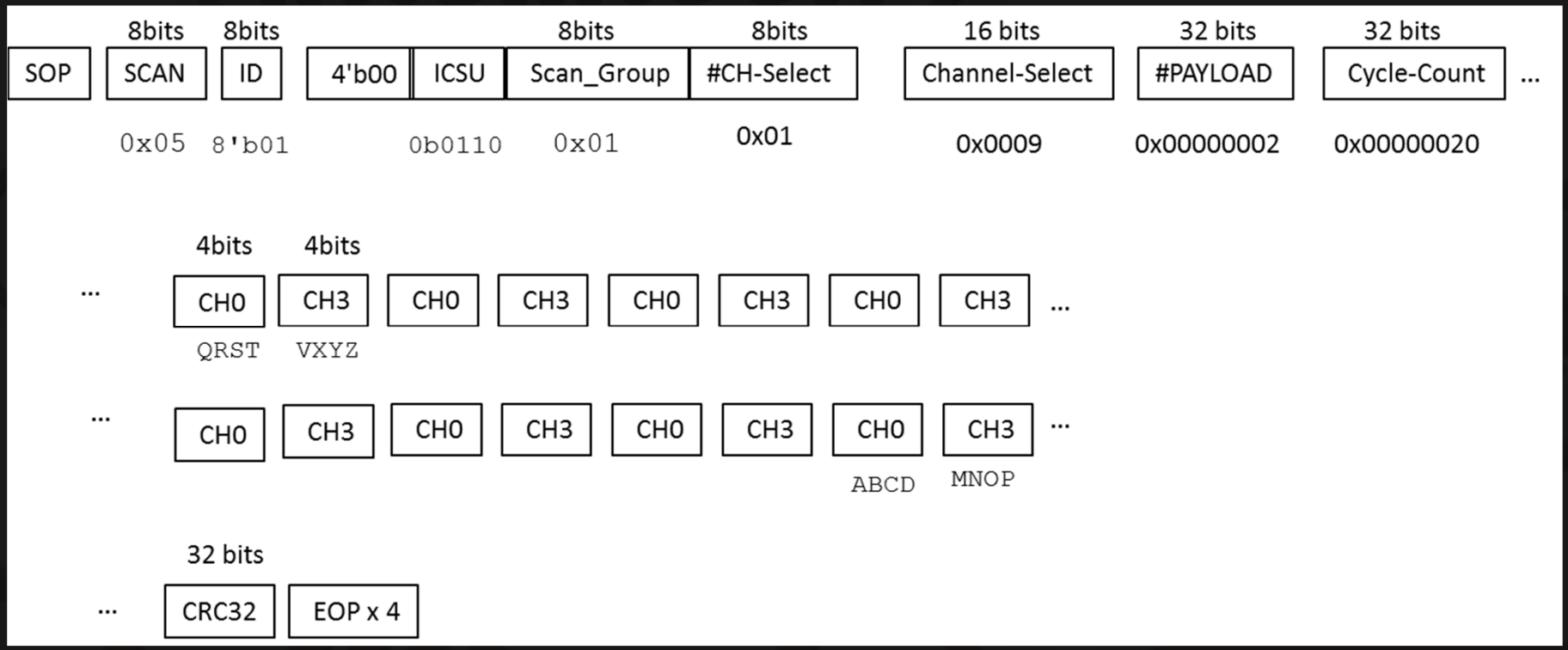
BOND - Bond multiple lanes together for increased bandwidth

All "R" response packets are ignored and forwarded to TX



SCAN Packet Delivers Scan data to SII

- Apply/Validate Test data
- Add instrument data to test data



PDL commands translated to P1149.10 Packets

```
# write to 8 AXI4 bus masters at the same time
iWrite AXI4[7::0]  0x11_22_33_44_55_66_77_88
# write scan data to 8 cores
iWrite Core[7:0].scan 0X11_22_33_44_55_66_77_88
# read temp in 16 places
iRead TEMP[15:0]
#  read VDD drop detectors in 16 places
iRead DroopDetector[15:0]
# send/receive data over SERDES
iApply
```

Conclusion

- P1149.10 is still in development
- Provides a baseline architecture for Silicon Debug
- High Bandwidth > 10Gb/sec
- More bandwidth means more possibilities
  for instrumentation used for Silicon Debug