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PRESS RELEASE

New software for Mentor Graphics Questa platform enables early verification of IEEE 1149.1-2013 compliant IP and on-chip Instruments

Dover, New Hampshire - April 22, 2014 — Intellitech announced today the availability of ISIS™, a simulation interface, which links Intellitech's on-chip debugger, NEBULA™, with the Mentor Graphics Questa® verification platform. IEEE 1149.1-2013 is the extensively revised version of the JTAG standard released by the IEEE in June of 2013 that adds hierarchical structural description languages for internal JTAG access and a hierarchical Procedure Definition Language (PDL). The IEEE 1149.1 standardized languages now replace ad-hoc approaches to instrument validation via Verilog test benches, test vectors, Perl and Python. The verification engineer can now validate the Verilog architecture of a wrapped instrument - an instrument with an IEEE 1149.1 test data register interface - for accuracy against the BSDL register descriptions and IEEE 1149.1 compliance. The engineer can also validate that the 1149.1-2013 PDL language (based on Tcl) operates the instrument as expected. Questa provides responses to the PDL based stimulus from NEBULA and ISIS and provides Verilog fault coverage reports that are critical to the validation. Once validated, the 1149.1-2013 based descriptions can be re-used at higher levels of integration in a SoC design. IC integrators can purchase IP and instruments with pre-validated descriptions and PDL that can plug and play into their IC design. The validated IEEE internal JTAG register descriptions and PDL can then be used during first silicon bring-up thus eliminating the debug of the created PDL against unproven hardware during the schedule's critical time.

"ISIS™ and NEBULA™ provide a powerful front end to Questa enabling IP providers to deliver pre-validated IEEE 1149.1 compliant SERDES I/O, BIST and Silicon Instruments™ to the IP provider's customer base pre-silicon," said CJ Clark, CEO of Intellitech Corporation and the IEEE 1149.1 Working Group chairperson. "SoC integrators can now specify validated IEEE 1149.1-2013 compliant interfaces and interface descriptions in BSDL and PDL as deliverables that their IP provider must provide," Clark added.

"Mentor is pleased to partner with Intellitech in support of the IEEE 1149.1-2013 standard through their ISIS interface to Questa," said Dennis Brophy, director of strategic business development, Mentor Graphics Corporation. "This integration supports early pre-silicon IP validation by using Questa in support of mutual customer demand for quicker and more predicable post-silicon bring-up."

NEBULA and ISIS for Questa are freely available software products for Questa and ModelSim® users with a valid business email address. See http://www.intellitech.com/ijtag.

A tutorial on the benefits of IEEE 1149.1-2013 can be found on Intellitech's website at http://www.intellitech.com/ijtag/ieee-1149-1-2013-tutorial-on-ijtag-instruments.pdf

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Acronyms and Definitions

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