Intellitech Corporation
69 Venture Drive
Dover, NH 03820
PH: (603) 750-7116

For more information, contact:
Kareen Lefoley
Tel. 603.750.7116x106
klefoley@intellitech.com

PRESS RELEASE

Intellitech Supports Silicon Instruments Through The New IEEE 1149.1-2013 JTAG Standard

Dover, New Hampshire - June 17, 2013 — Intellitech Corporation announced today support for accessing "Silicon Instruments" [SM] through the new IEEE 1149.1-2013 JTAG standard. The IEEE Standards Association announced the standard is available for purchase today. The new IEEE 1149.1-2013 includes structural and procedural description languages to support re-use of on-chip infrastructure IP or what Intellitech calls "Silicon Instruments." Examples of Silicon Instruments are: Memory BIST, I/O BIST, Logic BIST, SERDES PRBS, voltage droop monitors and temperature monitors. The hierarchical extensions to 1149.1 Boundary Scan Description Language (BSDL) allow self-contained Silicon Instrument descriptions to be supplied by the instrument provider in a new 'package' file format. These descriptions can then be instantiated and connected together via new capabilities of 1149.1-2013 that use the IEEE 1500 "Standard for Embedded Core Test" standard. Hierarchical documentation called Procedural Description Language (PDL), based on the open source Tcl, allows the Silicon Instrument vendor to describe the necessary steps to operate the instrument via the JTAG Test Access Port. An engineering manager's tutorial on the benefits of 1149.1-2013 can be found on Intellitech's website at 1149.1-2013 tutorial.

"Intellitech has been a pioneer in the use of 1149.1 with Silicon Instruments. We provided the fundamental groundwork in the late 1990s for many of the concepts now incorporated in 1149.1-2013 such as re-usable internal register definitions, mnemonics and the use of Tcl for JTAG test procedures. Until just a few years ago, many vendors were focused on just the boundary-scan half

of the 1149.1 standard," said CJ Clark, CEO of Intellitech Corporation and the IEEE 1149.1 Working Group chairperson.

"Naturally, Intellitech continues to maintain our leadership position with 1149.1-2013 support in our JAF® and PT100Pro production testers. We are also delighted that our business model enables us to offer NEBULA as a freely downloadable 1149.1-2013 software tool," Clark continued. "An engineer with a low cost USB based JTAG controller from an FPGA vendor and Intellitech's NEBULA software can start communicating with a chip in the lab, or start developing 1149.1-2013 packages for his or her own IP." Support is available for a nominal fee.

Intellitech's BERT-IP for SERDES BIST and DDR-IP for at-speed memory tests are available from Intellitech's Test-IP family of Silicon Instruments for FPGAs. Those instruments, introduced ten years ago, and upgraded with each FPGA generation, can now be operated on with 1149.1-2013 PDL. "FPGAs are uniquely 1149.1-2013 ready, as temporary Silicon Instruments can be downloaded and controlled through the 1149.1 TAP," Clark concluded.

Intellitech will be rapidly growing the use of 1149.1-2013 through a free web-based BSDL syntax and semantic checker compliant with the new standard at 1149.1-2013 BSDL Compiler. The freely available NEBULA product for accessing internal JTAG Silicon Instruments using 1149.1-2013 is available at Silicon Instruments. Engineers with a corporate email account can register on the website and download the software.

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